



Datasheet

DS000715

Mira130

1.3 MP NIR Enhanced Global Shutter CMOS Image Sensor

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Abstract

This datasheet document describes the specification and functionalities of Mira130, a 1.3 MP global shutter NIR image sensor with excellent Quantum Efficiency in the near-infrared range.

The main target application for this sensor is 3D-enabled consumer devices. The state-of-the-art NIR performance of Mira130 allows outstanding power consumption reduction of 3D systems in which this sensor is used.

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1 General Description

Mira130 is a global shutter CMOS image sensor with NIR enhancement of the QE. It outputs monochrome images with an effective pixel array of 1080 H x 1280 V, and supports complex on-chip operations such as high dynamic range (HDR) mode, external triggering, windowing, horizontal or vertical mirroring. Its maximum frame rate is 120 fps at a full image resolution. On-chip registers can be accessed via the standard I²C interface.

1.1 Key Benefits & Features

Figure 1:
Mira130 Key Benefits

Benefits	Features
State-of-the-art NIR performance	56% QE at 850 nm, 36% QE at 940 nm
HDR mode provides > 100 dB DR	In-pixel HDR mechanism
Motion blur robustness	Global shutter pixel
Standard camera interface	MIPI CSI-2 / D-PHY
High speed	Up to 120 fps @ 10-bit data
Optimized for size constrained applications	1.3 MP with 2.7 μm pixels

1.2 Other Features

- Support external triggering and multiple sensors synchronization
- AEC/AGC, minimum exposure time less than 1 line
- LED strobe
- Horizontal and vertical windowing
- 28x analog gain, and 32x digital gain
- High sensitivity
- Programmable registers through I²C
- Low power consumption
- Build-in temperature sensor

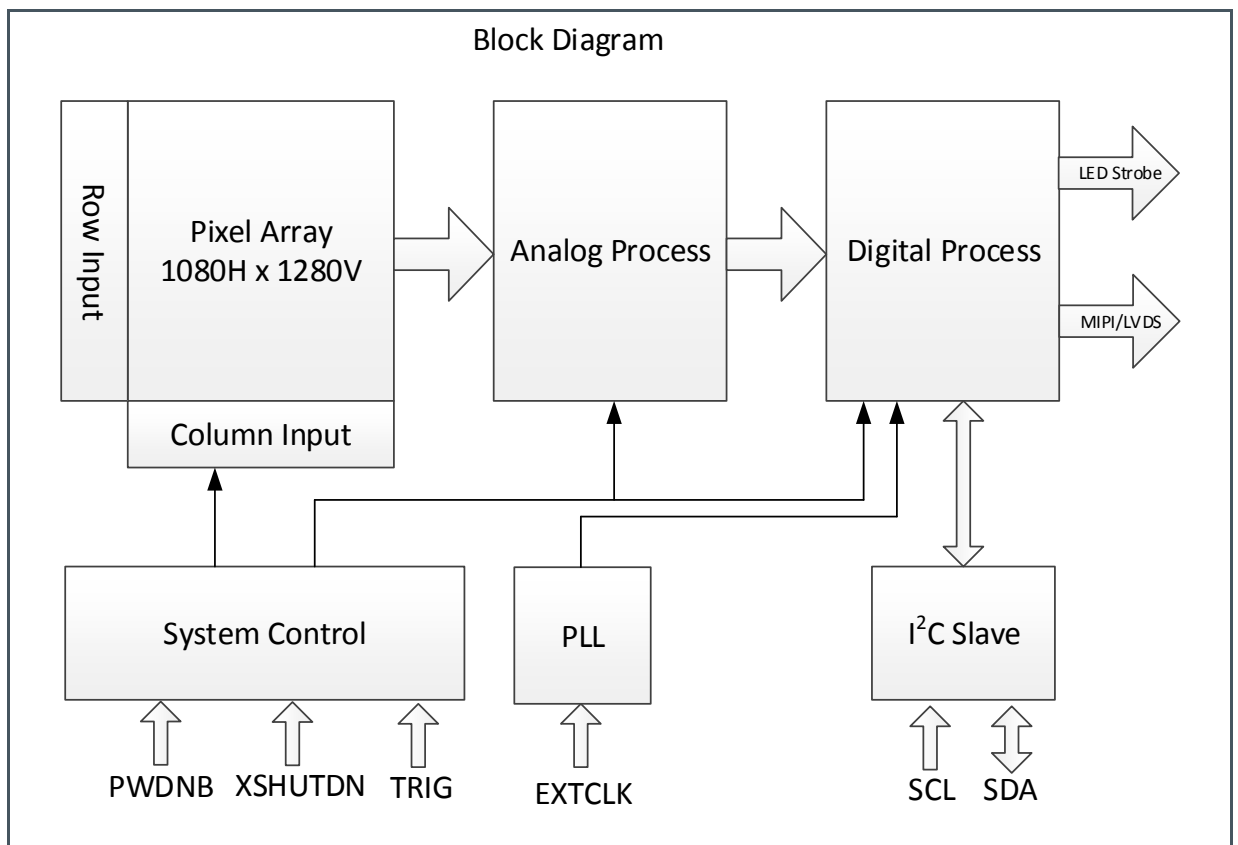
1.3 Applications

- 3D Structured light, 3D Active Stereo systems
- 2D NIR imaging
- Machine vision
- Barcode scanners
- Motion monitoring

1.4 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of Mira130



2 Ordering Information

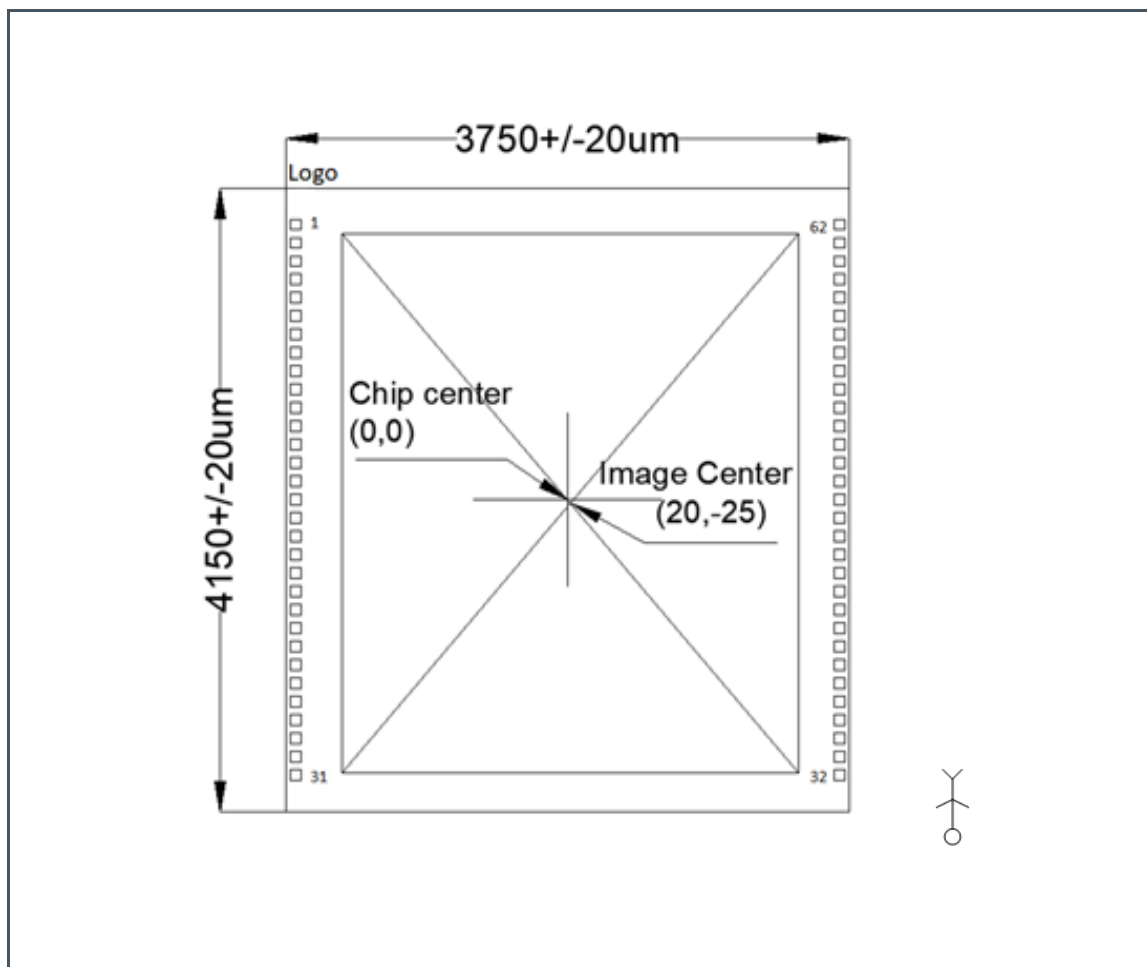
Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
MIRA130-1QM2D0	Bare die	N/A	Reconstructed wafer	1 wafer

3 Packaging Information

3.1 Mira130 Die Information

3.1.1 Mira130 Die Size

Figure 3:
Mira130 Die Pinout



- (1) The COB center of the chip is not coincident with the optical center. Pixel Center $(20,-25)$ is the same as the optical center. The units are in μm .

3.1.2 Mira130 Pad Description

Figure 4:
 Pad Description of Mira130 Die

Pad #	Pad Name	X-axis	Y-axis	Pin Type	Description
1	AVDD	-1791.5	1809	Power	2.5 V Analog Power Supply
2	AVDD	-1791.5	1688.4	Power	2.5 V Analog Power Supply
3	AGND	-1791.5	1567.8	GND	Analog Ground
4	ATM	-1791.5	1447.2	-	NC
5	DVDD	-1791.5	1326.6	Power	1.2 V Digital Power Supply
6	DVDD	-1791.5	1206	Power	1.2 V Digital Power Supply
7	DOGND	-1791.5	1085.4	GND	I/O Ground
8	DOGND	-1791.5	964.8	GND	I/O Ground
9	TRIGL/FSYNC	-1791.5	844.2	Input/ Output	External Triggering of HDR Long Exposure/SYNC
10	LEDSTROBE	-1791.5	723.6	Output	LED STROBE Signal
11	XSHUTDOWN	-1791.5	603	Input	XSHUTDOWN Signal Input (internal pull-up, active low)
12	TM	-1791.5	482.4	Input	Connect to the DOGND pin
13	AGND	-1791.5	361.8	GND	Analog Ground
14	AVDD	-1791.5	241.2	Power	2.5 V Analog Power Supply
15	TRIGS	-1791.5	120.6	Input	External Triggering of HDR Short Exposure
16	GPIO	-1791.5	0	-	NC
17	DOVDD	-1791.5	-120.6	Power	1.8 V I/O Power Supply
18	DOGND	-1791.5	-241.2	GND	I/O GROUND
19	AVDD	-1791.5	-361.8	Power	2.5 V Analog Power Supply
20	NC	-1791.5	-482.4	-	NC
21	VREFH	-1791.5	-603	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
22	NC	-1791.5	-723.6	-	NC
23	AVDD	-1791.5	-844.2	Power	2.5 V Analog Power Supply
24	AGND	-1791.5	-964.8	GND	Analog Ground
25	AGND	-1791.5	-1085.4	GND	Analog Ground
26	VREFN	-1791.5	-1206	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
27	VREFN1	-1791.5	-1326.6	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
28	GS_VREF	-1791.5	-1447.2	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
29	AVDD	-1791.5	-1567.8	Power	2.5 V Analog Power Supply
30	DVDD	-1791.5	-1688.4	Power	1.2 V Digital Power Supply
31	DOGND	-1791.5	-1809	GND	I/O GROUND

Pad #	Pad Name	X-axis	Y-axis	Pin Type	Description
32	DOGND	1791.5	-1809	GND	I/O GROUND
33	DVDD	1791.5	-1688.4	Power	1.2 V Digital Power Supply
34	MD3P	1791.5	-1567.8	Output	MIPI Data 3 Positive
35	MD3N	1791.5	-1447.2	Output	MIPI Data 3 Negative
36	DOGND	1791.5	-1326.6	GND	I/O GROUND
37	MD1P	1791.5	-1206	Output	MIPI Data 1 Positive
38	MD1N	1791.5	-1085.4	Output	MIPI Data 1 Negative
39	DVDD	1791.5	-964.8	Power	1.2 V Digital Power Supply
40	MCP	1791.5	-844.2	Output	MIPI Clock Positive
41	MCN	1791.5	-723.6	Output	MIPI Clock Negative
42	DOGND	1791.5	-603	GND	I/O Ground
43	DOGND	1791.5	-482.4	GND	I/O Ground
44	DOVDD	1791.5	-361.8	Power	1.8 V I/O Power Supply
45	DVDD	1791.5	-241.2	Power	1.2 V Digital Power Supply
46	MD0P	1791.5	-120.6	Output	MIPI Data 0 Positive
47	MD0N	1791.5	0	Output	MIPI Data 0 Negative
48	DOGND	1791.5	120.6	GND	I/O Ground
49	MD2P	1791.5	241.2	Output	MIPI Data 2 Positive
50	MD2N	1791.5	361.8	Output	MIPI Data 2 Negative
51	DVDD	1791.5	482.4	Power	1.2 V Digital Power Supply
52	DOVDD	1791.5	603	Power	1.8 V I/O Power Supply
53	SDA	1791.5	723.6	Input/ Output	I ² C Data Line (open drain)
54	DOGND	1791.5	844.2	GND	I/O Ground
55	SCL	1791.5	964.8	Input	I ² C Clock
56	EXTCLK	1791.5	1085.4	Input	Clock Input
57	SID0	1791.5	1206	Input	I ² C Device ID 0
58	SID1	1791.5	1326.6	Input	I ² C Device ID 1
59	DVDD	1791.5	1447.2	Power	1.2 V Digital Power Supply
60	DOGND	1791.5	1567.8	GND	I/O Ground
61	AGND	1791.5	1688.4	GND	Analog Ground
62	AVDD	1791.5	1809	Power	2.5 V Analog Power Supply

(1) All pads bonding area is 70 µm x 70 µm. Units are in µm.

3.2 RW (reconstructed wafer) Physical Dimensions

Max total die count: 8-inch: 1593 ea.

Film frame: Compact disco stainless SUS420

Carrier tape: UV tape

Figure 5:
RW Physical Dimensions

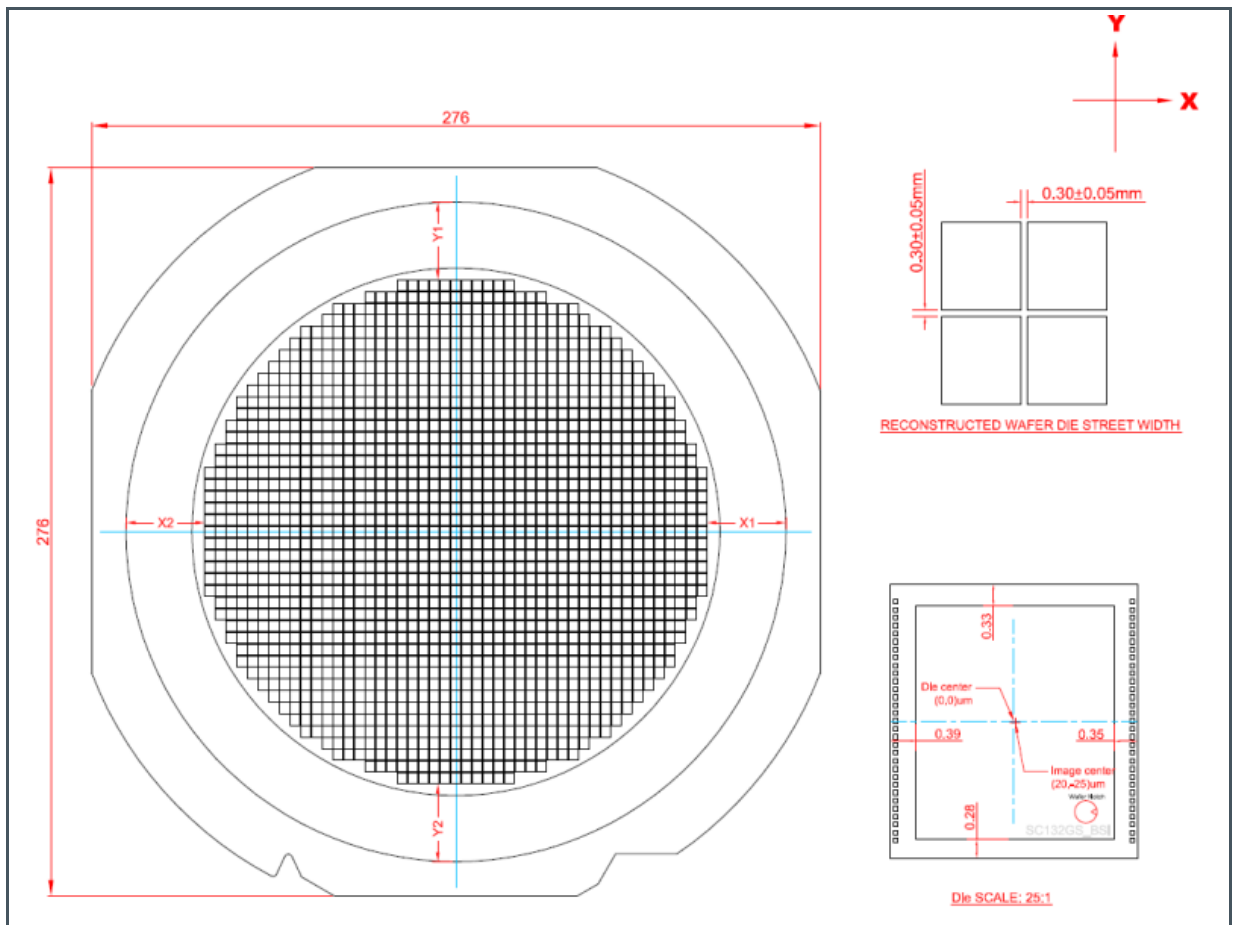


Figure 6:
Wafer Dimensions

Parameter	Description
Wafer Diameter	200 mm (8")
Grinding Thickness	150 µm ± 10 µm
Singulated Die Size	X = 3750 µm ± 20 µm, Y = 4150 µm ± 20 µm
Bond Pad Size	X = 80 µm, Y = 88 µm

Parameter	Description
Bond Pad Opening	X = 70 μm, Y = 70 μm
Minimum Bond Pad Pitch	120.6 μm
Optical Array (Optical center from die center)	X = 20 μm, Y = 25 μm
RW Offset	(X1 - X2) ÷ 2 = 0 ± 5 mm; (Y1 - Y2) ÷ 2 = 0 ± 5 mm;
Placement Accuracy X,Y,Theta	X, Y (±50 μm), Theta < 1°
Maximum Total Die Count	X, Y (±50 μm), Theta < 1°
RW Layout	X = 47, Y = 43

3.3 Mira130 Fan-Out Package (for information only)

3.3.1 Fan-Out Package Dimensions

The package drawing and dimensions are shown respectively on Figure 7 and Figure 8.

Figure 7:
Fan-Out Package Drawing

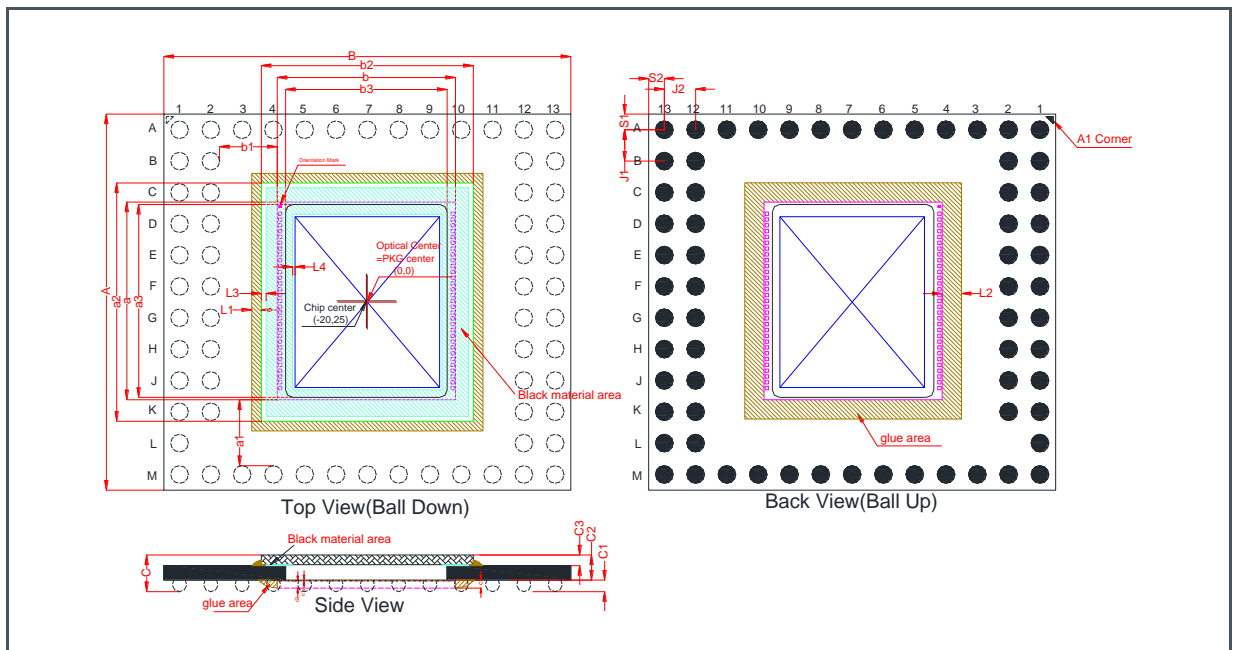


Figure 8:
Fan-Out Package Dimensions (in mm)

Parameters	Symbol	Nominal	Min	Max
Package Body Dimension Y	A	7.800	7.700	7.900
Package Body Dimension X	B	8.450	8.350	8.550
Package Height	C	0.810	0.725	0.895
Ball Height	C1	0.290	0.255	0.325
Package Body Thickness	C2	0.520	0.470	0.570
Glass Thickness(with glue thickness)	C3	0.220	0.210	0.230
Ball Diameter	D	0.365	0.330	0.400
Die Body Dimension Y	a	4.100	NA	NA
Die Edge To Ball Edge Dimension Y	a1	1.368	1.343	1.393
Glass Package Body Dimension Y	a2	4.942	4.917	4.967

Parameters	Symbol	Nominal	Min	Max
Slot Opening Dimension Y	a3	4.000	NA	NA
Die Body Dimension X	b	3.700	NA	NA
Die Edge To Ball Edge Dimension X	b1	1.198	1.173	1.223
Glass Package Body Dimension X	b2	4.402	4.377	4.427
Slot Opening Dimension X	b3	3.353	NA	NA
Die Package Height	c	0.167	0.152	0.182
Si Thickness	c2	0.150	0.140	0.160
Gold Bump Height	c1	0.017	0.012	0.022
Gold Bump Diameter	d	0.075	0.070	0.080
Glue Area Width(Top)	L1	NA	NA	0.200
Glue Area Width(Bottom)	L2	NA	NA	0.400
Total Ball Count	N	65 (6NC)		
Ball Pitch Y axis	J1	0.650		
Ball Pitch X axis	J2	0.650		
Edge to Ball Center Distance along Y	S1	0.325	0.250	0.400
Edge to Ball Center Distance along X	S2	0.325	0.250	0.400

(1) The center of the fan-out package is coincident with the optical center.

3.3.2 Fan-Out Package Pin List

Figure 9:
Fan-Out Pin Description

#	Pin #	Pin Name	Pin Type	Description
1	A1	NC	-	NC
2	A2	DVDD	Power	1.2 V Digital Power Supply
3	A3	ATM	-	NC
4	A4	DOGND	GND	Analog/Digital GND
5	A5	AVDD	Power	2.5 V Analog Power Supply
6	A6	AVDD	Power	2.5 V Analog Power Supply
7	A7	DOGND	GND	Analog/Digital GND
8	A8	DOGND	GND	Analog/Digital GND
9	A9	DVDD	Power	1.2 V Digital Power Supply
10	A10	SID1	Input	I ² C Device ID 1

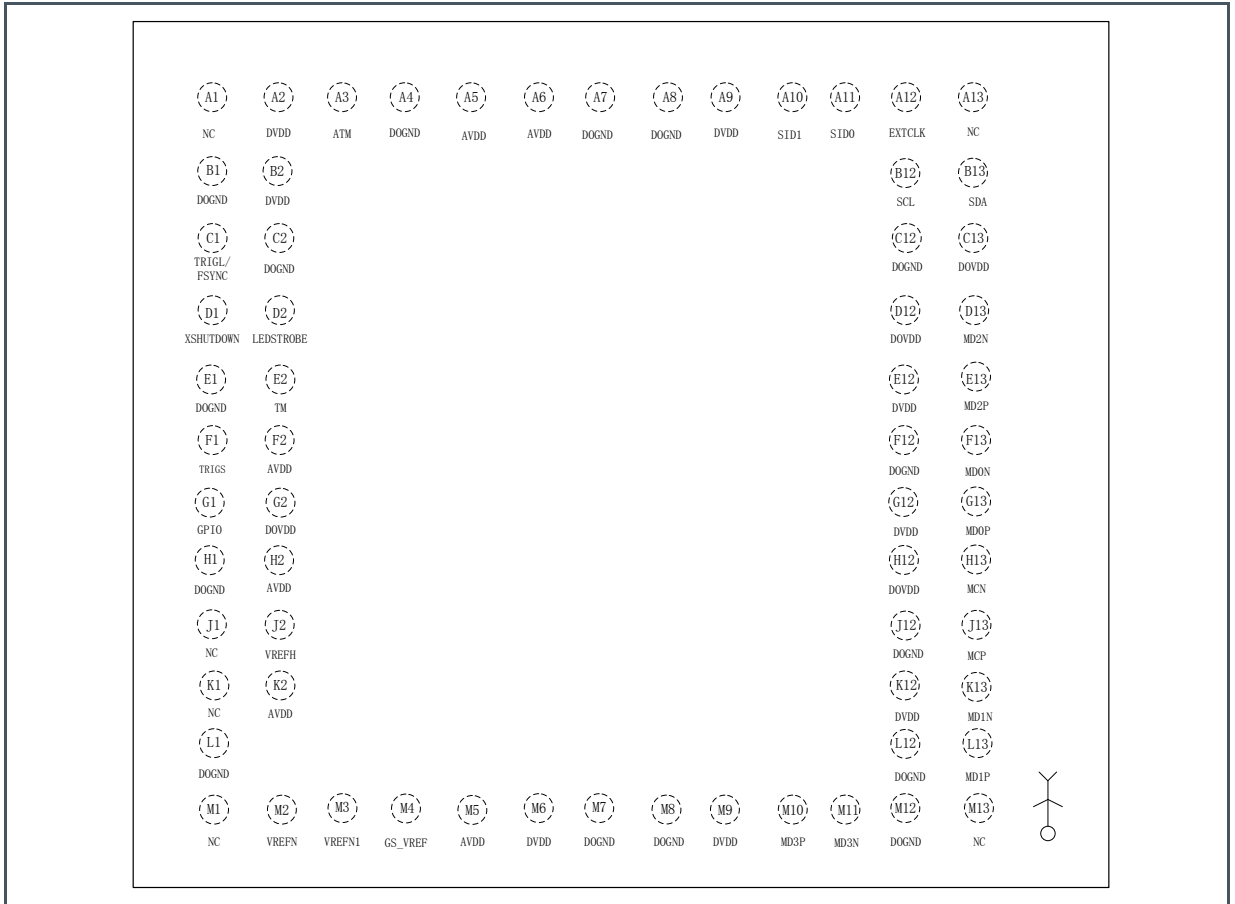
#	Pin #	Pin Name	Pin Type	Description
11	A11	SID0	Input	I ² C Device ID 0
12	A12	EXTCLK	Input	Clock Input
13	A13	NC	-	NC
14	B1	DOGND	GND	Analog/Digital GND
15	B2	DVDD	Power	1.2 V Digital Power Supply
16	B12	SCL	Input	I2C Clock
17	B13	SDA	Input/Input	I2C Data Line (open drain)
18	C1	TRIGL/FSYNC	Input/Input	External Triggering of HDR Long Exposure/SYNC
19	C2	DOGND	GND	Analog/Digital GND
20	C12	DOGND	GND	Analog/Digital GND
21	C13	DOVDD	Power	1.8 V I/O Power Supply
22	D1	XSHUTDOWN	Input	XSHUTDOWN Signal Input (internal pull-up, active low)
23	D2	LEDSTROBE	Output	LED STROBE Signal
24	D12	DOVDD	Power	1.8 V I/O Power Supply
25	D13	MD2N	Output	MIPI Data 2 Negative
26	E1	DOGND	GND	Analog /Digital GND
27	E2	TM	Input	Connect to DOGND pin
28	E12	DVDD	Power	1.2 V Digital Power Supply
29	E13	MD2P	Output	MIPI Data 2 Positive
30	F1	TRIGS	Input	External Triggering of HDR Short Exposure
31	F2	AVDD	Power	2.5 V Analog Power Supply
32	F12	DOGND	GND	Analog /Digital GND
33	F13	MD0N	Output	MIPI Data 0 Negative
34	G1	GPIO	-	NC
35	G2	DOVDD	Power	1.8 V I/O Power Supply
36	G12	DVDD	Power	1.2 V Digital Power Supply
37	G13	MD0P	Output	MIPI Data 0 Positive
38	H1	DOGND	GND	Analog GND/Digital GND
39	H2	AVDD	Power	2.5 V Analog Power Supply
40	H12	DOVDD	Power	1.8 V I/O Power Supply
41	H13	MCN	Output	MIPI Data Clock Negative
42	J1	NC	-	NC

#	Pin #	Pin Name	Pin Type	Description
43	J2	VREFH	Output	Internal Reference Voltage (connect an external capacitor to the DOGND pin)
44	J12	DOGND	GND	Analog /Digital GND
45	J13	MCP	Output	MIPI Data Clock Positive
46	K1	NC	-	NC
47	K2	AVDD	Power	2.5 V Analog Power Supply
48	K12	DVDD	Power	1.2 V Digital Power Supply
49	K13	MD1N	Output	MIPI Data 1 Negative
50	L1	DOGND	GND	Analog/Digital GND
51	L12	DOGND	GND	Analog/Digital GND
52	L13	MD1P	Output	MIPI Data 1 Positive
53	M1	NC	-	NC
54	M2	VREFN	Output	Internal Reference Voltage (connect an external capacitor to the DOGND pin)
55	M3	VREFN1	Output	Internal Reference Voltage (connect an external capacitor to the DOGND pin)
56	M4	GS_VREF	Output	Internal Reference Voltage (connect an external capacitor to the DOGND pin)
57	M5	AVDD	Power	2.5 V Analog Power Supply
58	M6	DVDD	Power	1.2 V Digital Power Supply
59	M7	DOGND	GND	Analog GND/Digital GND
60	M8	DOGND	GND	Analog GND/Digital GND
61	M9	DVDD	Power	1.2 V Digital Power Supply
62	M10	MD3P	Output	MIPI Data 3 Positive
63	M11	MD3N	Output	MIPI Data 3 Negative
64	M12	DOGND	GND	Analog/Digital GND
65	M13	NC	-	NC

3.3.3 Fan-Out Package Pin Diagram

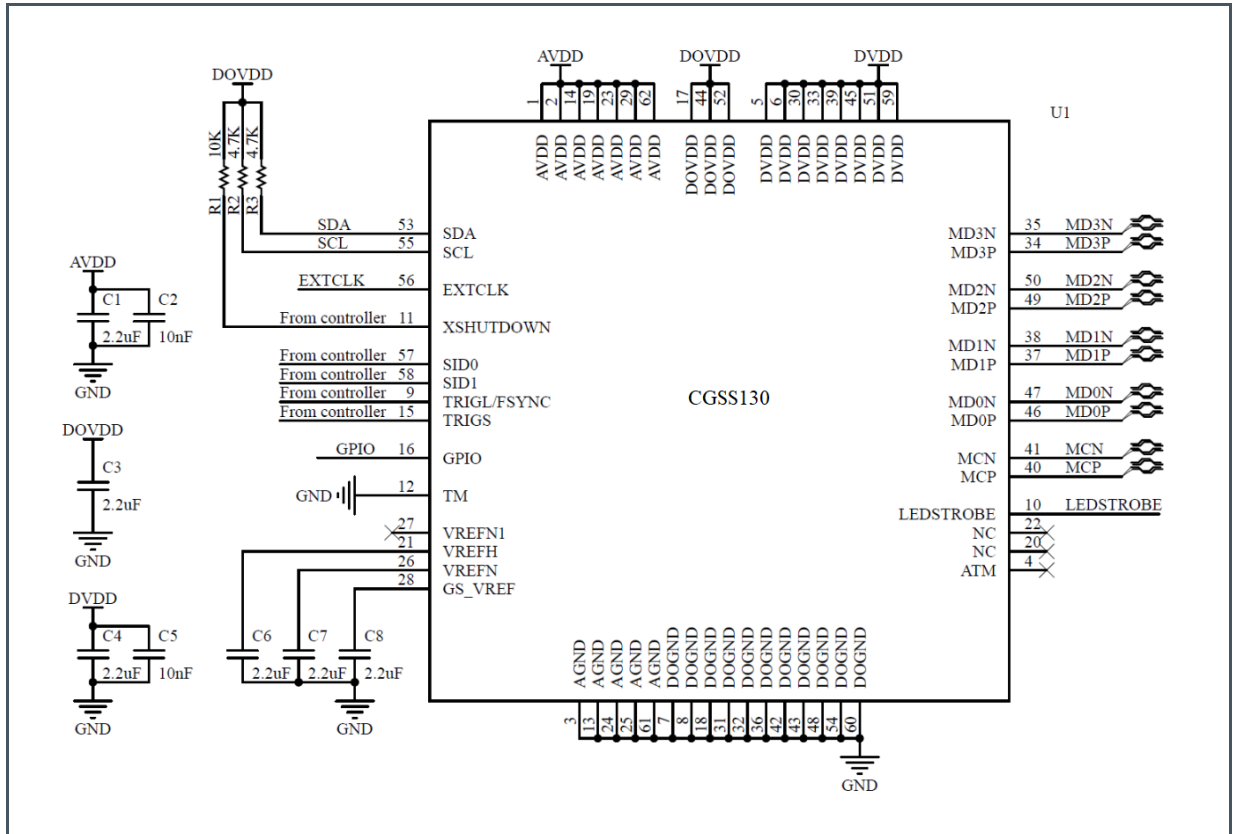
The following Figure 10 shows the pin assignment of Mira130.

Figure 10:
Fan-Out Pin Assignment



4 Typical Application Circuit

The typical application circuit of Mira130 using the MIPI interface is shown below.



- (1) The chip requires 3 power supplies: The AVDD pin shall be externally connected to a 2.5 V power supply, the DOVDD pin shall be externally connected to a 1.8 V power supply, and the DVDD pin shall be externally connected to a 1.2 V power supply. Filter capacitors shall be placed close to the corresponding pins. The capacitor values can be found in the figure above.
- (2) The GS_VREF, VREFN, VREFH pins shall be externally connected to ground through a 2.2 μ F capacitor which is close to the corresponding pin but kept as far as possible from the I/O signals such as EXTCLK, TRIG, MIPI differential pairs.
- (3) The active low XSHUTDN pin is controlled by an external main control chip. It shall be connected to the DOVDD pin through a 10 k Ω pull-up resistor.
- (4) The external clock signal can be generated by a crystal connecting to the EXTCLK pin, or provided by an external ISP/MCU, applying directly to the EXTCLK pin.
- (5) The analog ground and the digital ground are recommended to be connected directly.
- (6) The SID0 and SID1 pins shall be either pulled up to the DOVDD pin or pulled down to the AGND pin, but shall never be floating.
- (7) The requirements of routing MIPI differential pairs areas follows:
 - a) The control standard of the impedance of MIPI differential pairs is 100 Ω , and the tolerance is limited to $\pm 10\%$.
 - b) The differential pairs should not be right-angled in order to avoid reflections, and as a result affect high-speed transmission performance.
 - c) Reference layer: There must be a reference layer below the MIPI differential pairs (a ground plane is recommended). The continuity of the layer must be guaranteed, that is the layer below the MIPI differential pairs cannot be fragmented, cannot consist of gaps, and cannot be cut by other lines. A whole layer of ground is preferred. If not possible, the minimum requirement is to ensure that the reference layer below the MIPI differential pairs is 4 W wider than each side of the MIPI signal wire, where W is the width of MIPI differential pairs.

- d) Equal length:** The difference in length between the two wires of a MIPI differential pair should be limited to 10 mils, and the difference in length among MIPI differential pairs should be controlled within 100 mils. These requirements ensure that the differential signals can reach the receiving end at the same time. When implementing the requirement of equal length, the symmetry should be considered. The distance between meander wires should be 4 times the trace width to avoid being too dense. The wires should be wound near the bonding pad as much as possible to keep equal length, and the wire width and distance cannot be changed arbitrarily.
- e) Symmetry:** MIPI differential pairs should be kept equal length and distance. The purpose of symmetry is to ensure the consistency of trace impedance in order to reduce reflection. Poor symmetry may result in signal distortion, instability or no image.
- f) Keep clear of interference:** The clearance between MIPI differential pairs should be larger than $2W$. The clearance between MIPI differential pairs and other high-speed signals (parallel data lines, clock lines, etc.) should be larger than $3W$, and they should not be routed in parallel. A larger clearance should be considered to avoid interference generated from circuits such as switching power supplies.
- g) Through holes:** Through holes should be avoided for MIPI differential pairs. If unavoidable, through holes should be on both wires of the differential pair in order to maintain symmetry. If a differential pair is routed to another layer by means of through holes, the reference layer should also follow by means of through holes near the through holes of the differential pair.

5 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 11:
Absolute Maximum Ratings of Mira130

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V _{AVDD}	Analog Supply Voltage	-0.3	3.0	V	
V _{DOVDD}	I/O Supply Voltage	-0.3	2.2	V	
V _{DVDD}	Digital Supply Voltage	-0.3	1.4	V	
	I/O Input Voltage	-0.3	V _{DOVDD} + 0.3	V	
	I/O Output Voltage	-0.3	V _{DOVDD} + 0.3	V	
I _{SCR}	Input Current (latch-up immunity)	± 200		mA	JEDEC JESD78E Nov 2016
Electrostatic Discharge					
ESD _{HBM}	Electrostatic Discharge HBM		± 3.5	kV	MIL-STD-883J Method 3015.9
ESD _{CDM}	Electrostatic Discharge CDM		± 2	kV	ANSI/ESDA/JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
T _A	Operating Ambient Temperature	-30	85	°C	
T _{SPEC}	Operating Temperature Spec	-20	60	°C	
T _J	Operating Junction Temperature	-25	90	°C	
T _{STRG_WAF}	Storage Temperature Range Wafer	20	30	°C	
t _{STRG_WAF}	Storage Time Wafer		6	months	
RH _{NC_WAF}	Relative Humidity (non-condensing) Wafer		30	%	N2 Wafer Stocker condition ¹

¹ Die and wafers, when in storage, should be stored at temperature between 20°C and 30°C, relative humidity of less than 30%, and in clean, dry, inert atmosphere (e.g. Nitrogen) or in a vacuum sealed bag.

Symbol	Parameter	Min	Max	Unit	Comments
MSL _{DIE}	Moisture Sensitivity Level bare die		N/A		

6 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 12:
DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
V_{AVDD}	Analog supply voltage		2.4	2.5	2.6	V
V_{DOVDD}	I/O supply voltage		1.7	1.8	1.9	V
V_{DVDD}	Digital supply voltage		1.14	1.2	1.26	V
I_{AVDD}	Analog supply current	@ 120 fps	-	23 ⁽¹⁾		mA
I_{DOVDD}	I/O supply current	@ 120 fps	-	0.5 ⁽¹⁾		mA
I_{DVDD}	Digital supply current	@ 120 fps	-	49 ⁽¹⁾		mA
P_{tot}	Total power consumption	@ 120 fps	-	117 ⁽¹⁾		mW
I_{AVDD}	Analog supply current	@ 60 fps	-	23 ⁽¹⁾		mA
I_{DOVDD}	I/O supply current	@ 60 fps	-	0.5 ⁽¹⁾		mA
I_{DVDD}	Digital supply current	@ 60 fps	-	33 ⁽¹⁾		mA
P_{tot}	Total power consumption	@ 60 fps	-	97.14 ⁽¹⁾		mW
Digital Input (Reference: AVDD = 2.5 V, DOVDD = 1.8 V)						
V_{IL}	Input low level		-	-	$0.3 \times V_{DOVDD}$	V
V_{IH}	Input high level		$0.7 \times V_{DOVDD}$	-	-	V
C_{IN}	Input capacitor		-	-	10	pF
Digital Output (25 pF standard load)						
V_{OH}	Output high level		$0.9 \times V_{DOVDD}$	-	-	V
V_{OL}	Output low level		-	-	$0.1 \times V_{DOVDD}$	V
Serial Interface Input (SCL and SDA)						
V_{IL}	Input low level		-0.5	0	$0.3 \times V_{DOVDD}$	V

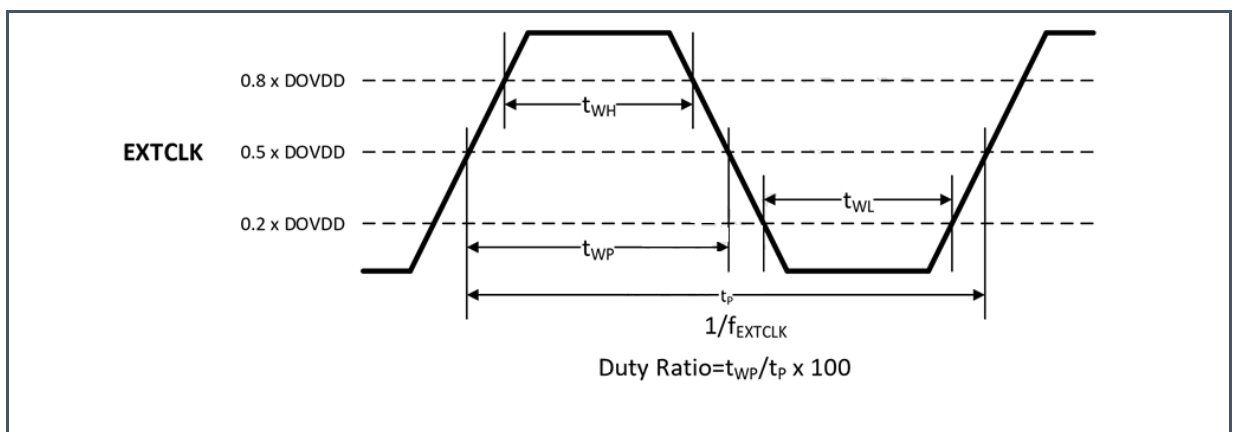
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level		$0.7 \times V_{DOVDD}$	V_{DOVDD}	$V_{DOVDD} + 0.5$	V

(1) Condition : MIPI:4lane_607.5 Mbit/s, Bitwidth:10-bit, Resolution:1080x1280

Figure 13:
AC Characteristics (T = 25 °C, $V_{AVDD} = 2.5$ V, $V_{DOVDD} = 1.8$ V)

Symbol	Parameter	Min	Typ	Max	Unit
AC Parameters					
DLE	DC differential linearity deviation	-	< 1	-	LSB
ILE	DC integral linearity deviation	-	< 2	-	LSB
	Soft reset settling time	-	-	1	ms
	Resolution change settling time	-	-	1	ms
	Register initialization time	-	-	300	ms
Crystal and Clock Input					
f_{extclk}	Input clock frequency	6	-	27	MHz
	Input clock rise/fall time	-	-	5	ns

Figure 14:
Input Clock Waveform



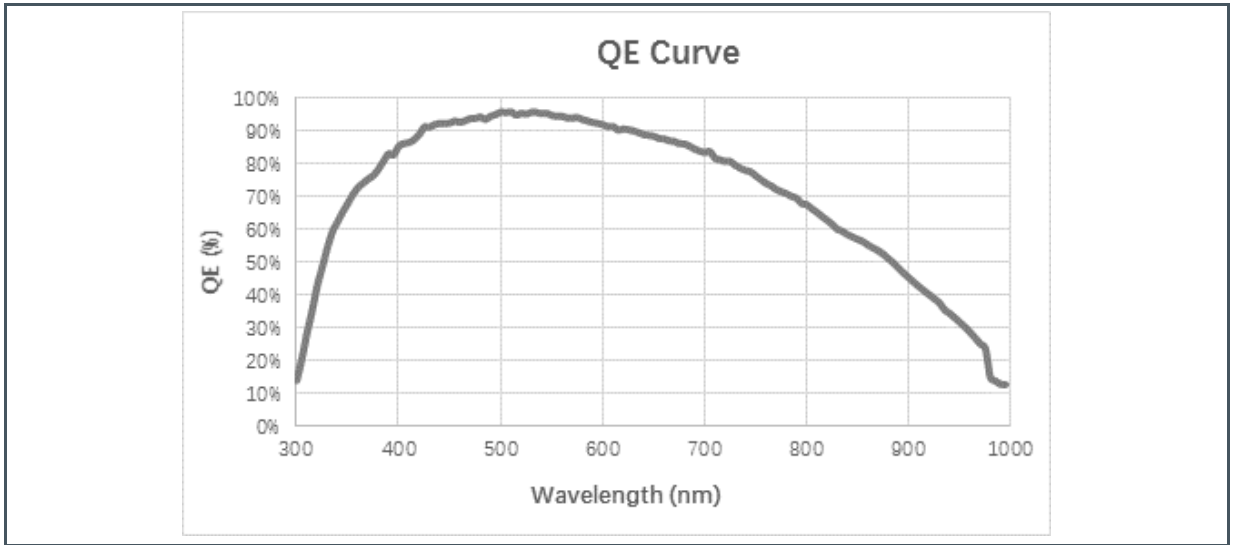
7 Electro-Optical Characteristics

This section shows the typical electro-optical characteristics of Mira130, measured in typical conditions.

Figure 15:
Electro-Optical Characteristics of Mira130

Parameter	Value	Remark
Active pixels	1080 (H) x 1280 (V)	
Pixel size	2.7 x 2.7 μm^2 BSI	
Pixel type	Voltage Domain Global Shutter	
Optical format	1/4"	
Full well charge	9 ke-	Linear full well
Temporal noise	< 8 e-	
Dynamic range	57 dB in normal mode 100 dB in HDR mode	In-pixel HDR allows exceptional performance
SNR	40 dB	
PLS	1/7500	
Responsivity	7000 mV/lux*s	
Quantum efficiency in NIR	58% at 850 nm 36% at 940 nm	See QE measurement curve below
Maximum frame rate	Non-HDR: 1080 H x 1280 V @10-bit 120 fps HDR (HDRC on): 1080 H x 1280 V @10-bit <60 fps HDR (HDRC off): 1080 H x 1280 V @10-bit 120 fps	
Output interface	10/8-bit 4lane MIPI 10/8-bit 4lane LVDS	
Output format	RAW / MONO	
CRA	25 degree	

Figure 16:
QE Measurement Curve



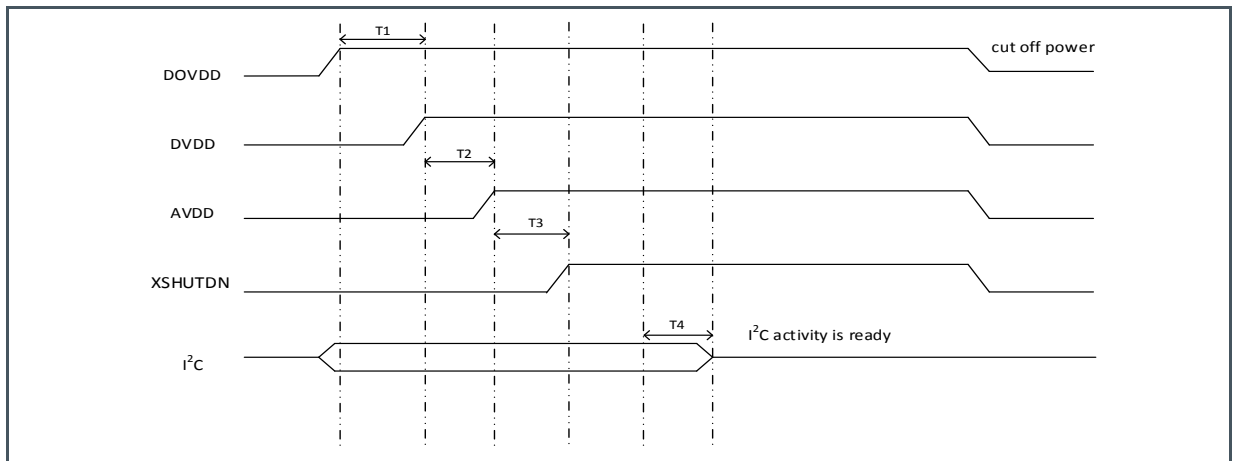
8 Functional Description

8.1 Chip Description

8.1.1 Power-On Sequence

With an external supply of 1.2 V to DVDD, the following power-on sequence is required:

Figure 17:
Power-Up Sequence



(1) $T1 > 0 \text{ ms}$, $T2 > 1 \text{ ms}$, $T3 > 2 \text{ ms}$, $T4 > 2 \text{ ms}$

8.1.2 I/O Pins Power-On Status

Figure 18:
Pins Power-On Status

Pin Name	Built-In Pull-Up/Pull-Down	Power Stable and XSHUTDOWN Low	XSHUTDOWN High
TRIGS	No	High-Z	Low
FSYNC	No	High-Z	Low
LED STROBE	No	High-Z	Low
GPIO	No	High-Z	Low

8.1.3 Sleep Mode

Under sleep mode, this chip stops output data, works in a low power status, and keeps registers unchanged. This chip enters sleep mode by writing 0 to register 16'h0100[0]. I²C access remains active:

Figure 19:
Sleep Mode Control Register

Function	Address	Default Value	Description
Sleep mode	16'h0100	1'b1	Bit[0]: Manual sleep mode control 0: Sleep mode enable 1: Sleep mode disable

8.1.4 Reset Mode

During reset, this chip stops outputting data, stays in sleep mode by the software approach, and resets its registers to their default values. This chip offers two approaches to reset:

1. Hard reset: Pull the XSHUTDN pin low, I²C read and write are not supported.
2. Soft reset: Write 1 to register 16'h0103[0], reset mode lasts for 150 ns

Figure 20:
Soft Reset Control Register

Function	Address	Default Value	Description
Soft reset	16'h0103	1'b0	Bit[0]: Soft reset

8.2 Configuration Interface

The on-chip registers can be read and written through the standard I²C interface. The device address of the I²C interface is determined by the SID0 and SID1 pins as shown in Figure 21.

Figure 21:
I²C Bus Device Address Control

7-bit I ² C Bus Device Address	SID0	SID1
7'h30	Low	Low
7'h31	High	Low
7'h32	Low	High
7'h33	High	High

In the example below, the first line below shows a standard I²C communication protocol for 7-bit slave address, 16-bit sub address and 8-bit data. The slave address is the I²C bus device address, which is 7-bit. The R/W bit is either 1 for read or 0 for write. The 2 sub address bytes are the high byte and low byte of the 16-bit address of the register to be accessed.

The second line in the example shows a write operation.

The third line shows a read operation. A dummy write operation is required to set the sub address (i.e. register address) before the read operation.



Information

16-bit register address, 8-bit data, 7-bit device address

Figure 22:
I²C Bus Device Address Control Example

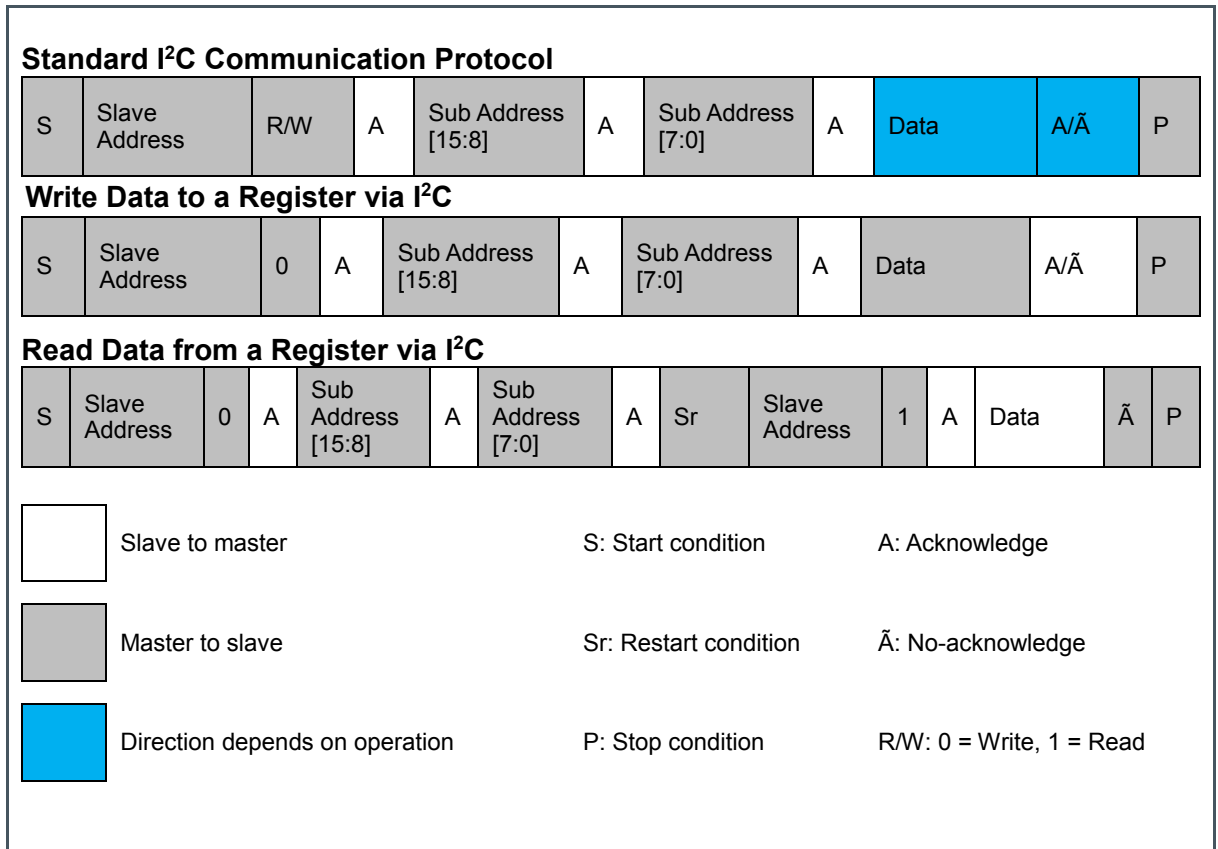
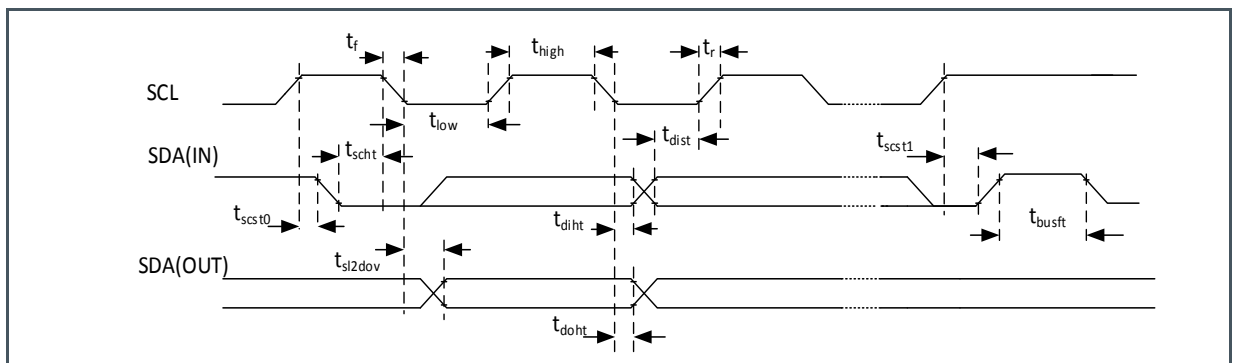


Figure 23 shows the I²C interface timing diagram.

Figure 23:
I²C Interface Timing



- (1) I²C interface timing is based on a 400 kHz mode.
- (2) The beginning of a rising edge and the end of a falling edge are at 10% of the amplitude of the signal. The end of a rising edge and the beginning of a falling edge are at 90% of the amplitude of the signal.

Figure 24:
I²C Interface Timing Parameter

Symbol	Parameter	Min	Typical	Max	Unit
f _{I2C}	Clock frequency	—	—	400	kHz
t _{low}	Clock low period	1.3	—	—	μs
t _{high}	Clock high period	0.6	—	—	μs
t _{sl2dov}	SCL low to data out valid	0.1	—	0.9	μs
t _{busft}	Bus free time before new start	1.3	—	—	μs
t _{scht}	Start condition hold time	0.6	—	—	μs
t _{scst0}	Start condition setup time	0.6	—	—	μs
t _{dih}	Data in hold time	0	—	—	μs
t _{dist}	Data in setup time	0.1	—	—	μs
t _{scst1}	Stop condition setup time	0.6	—	—	μs
t _r	Rise time	—	—	0.3	μs
t _f	Fall time	—	—	0.3	μs
t _{doht}	Data out hold time	0.05	—	—	μs

8.3 Sensor ID

Figure 25:
Sensor ID Registers

Function	Address	Default Value
Sensor ID high byte	16'h3107	8'h01
Sensor ID low byte	16'h3108	8'h32

8.4 Data Interface

There are 2 types of data interfaces in this chip: the Mobile Industry Processor Interface (MIPI), and the Low Voltage Differential Signaling (LVDS). Only MIPI interface documentation is provided hereunder. For information on LVDS, please request this to your **ams** contact.

8.4.1 Mobile Industry Processor Interface (MIPI)

This chip provides a Mobile Industry Processor Interface (MIPI), which supports 8/10/12-bit, 1/2/4-lane data serial output with a speed of lower than 1.25 Gbit/s per lane. Figure 26 shows the MIPI interface.

Figure 26:
MIPI Interface

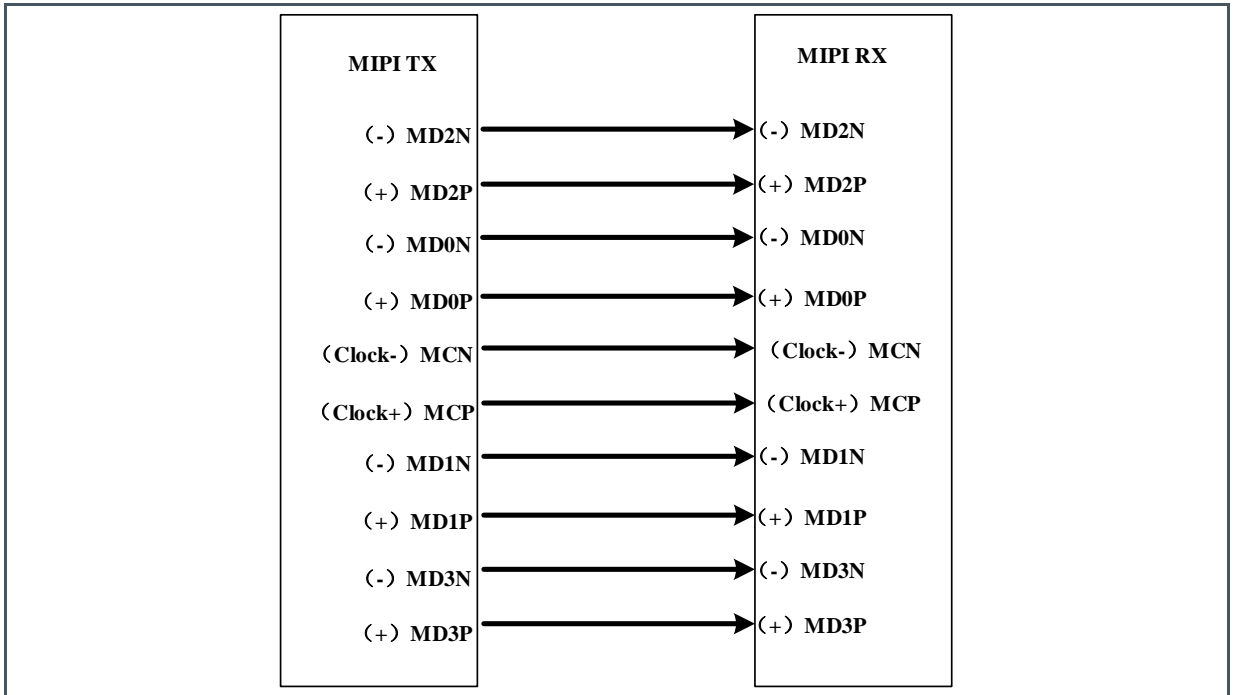


Figure 27 shows an example of low-level MIPI data packet, and more specifically the transmission sequence of a short packet followed by a long packet.

Figure 27:
MIPI Low Level Data Packet

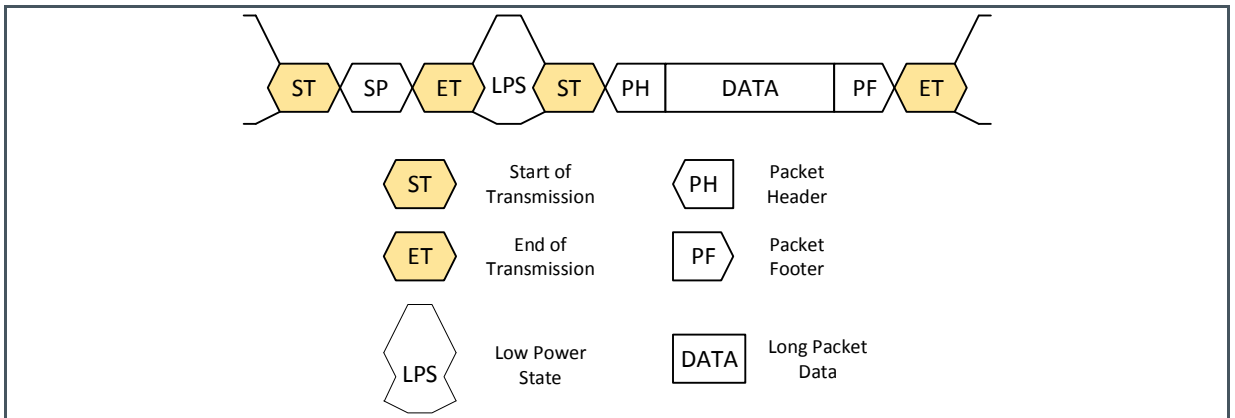


Figure 28 shows the different data types that can be used in a MIPI transmission. The diagram on Figure 29 shows the MIPI long/short packet structure. The Data Identifier (DI) is used to identify different packet types.

Figure 28:
MIPI Data Types

Data Type	Description
6'h00	Frame start short packet
6'h01	Frame end short packet
6'h02	Row start short packet
6'h03	Row end short packet
6'h2a	8-bit data long packet
6'h2b	10-bit data long packet
6'h2c	12-bit data long packet

Figure 29:
MIPI Long & Short Packet Structure Diagrams

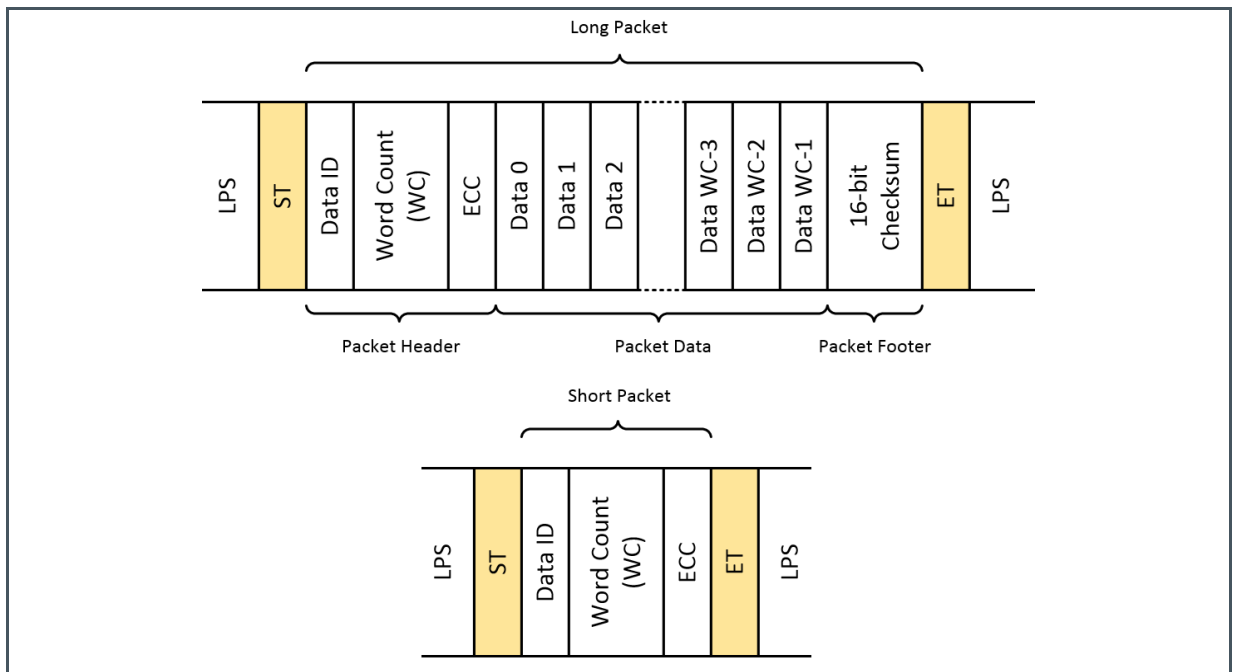


Figure 30 shows the data packet transmission diagram of the MIPI working in 1-lane, 2-lane and 4-lane. In Figure 31, we learn that DI consists of two parts, Virtual Channel (VC) and Data Type (DT). By default, the MIPI data VC value given by this chip is 0, and values of DT are shown in Figure 28.

Figure 30:
MIPI 1/2/4-Lane Data Package Transmission

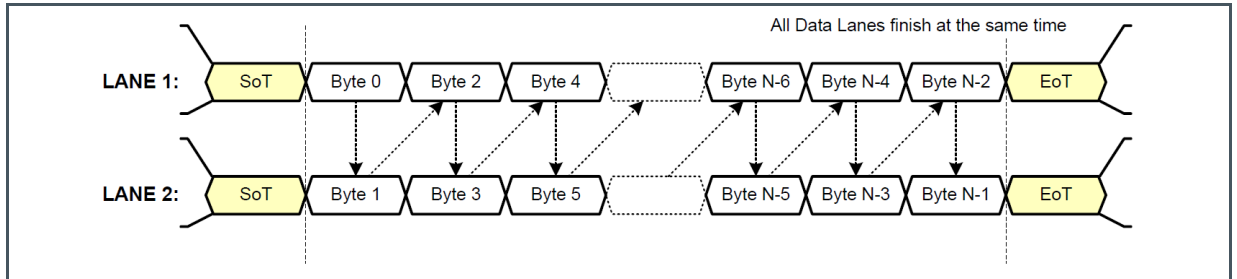
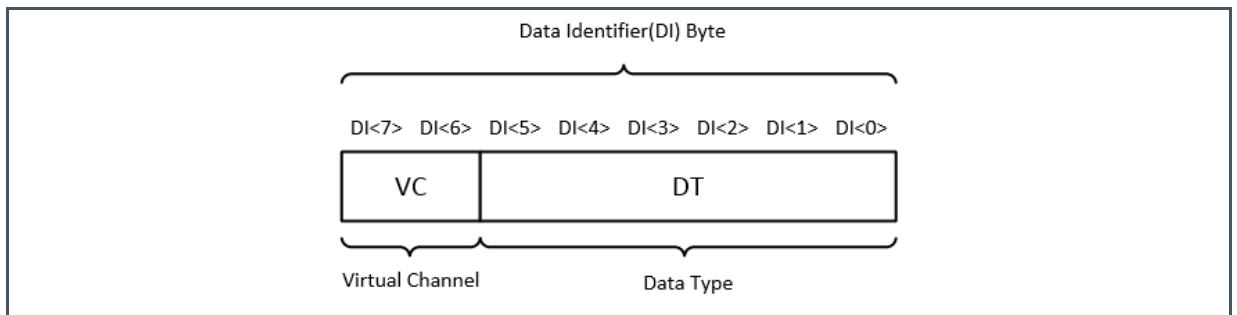


Figure 31:
MIPI Data Packet DI Structure



Other useful MIPI control registers can be found below.

Figure 32:
MIPI Control Registers

Function	Address	Default Value	Description
MIPI lane number	16'h3018	8'h72	Bit[7:5]: MIPI lane number 3'h0: 1-lane mode 3'h1: 2-lane mode 3'h3: 4-lane mode
MIPI output data mode	16'h3031	8'h0a	Bit[3:0]: MIPI bit mode 4'h8: raw8 mode 4'hc: raw12 mode Others: raw10 mode
PHY data mode	16'h3037	8'h00	Bit[6:5]: PHY bit mode 2'h0: 8-bit mode 2'h1: 10-bit mode 2'h2: 12-bit mode
MIPI clock setting	16'h303f	8'h01	Bit[7]: pclk sel 1'h0: sel pll_pclk
MIPI driving	16'h3651	8'h7d	Bit[3:0]: MIPI driving capability, the default value is 4'hd

Function	Address	Default Value	Description
MIPI Lane 0 delay	16'h3652	8'h00	Bit[3]: Lane 0 invert, the default value is 1'h0 Bit[2:0]: Delay of lane 0 equals to the value of bit[2:0] × 40 ps, the default value is 3'h0
MIPI Lane 1 delay	16'h3652	8'h00	Bit[7]: Lane 1 invert, the default value is 1'h0 Bit[6:4]: Delay of lane 1 equals to the value of bit[6:4] × 40 ps, the default value is 3'h0
MIPI Lane 2 delay	16'h3653	8'h00	Bit[3]: Lane 2 invert, the default value is 1'h0 Bit[2:0]: Delay of lane 2 equals to the value of bit[2:0] × 40 ps, the default value is 3'h0
MIPI Lane 3 delay	16'h3653	8'h00	Bit[7]: Lane 3 invert, the default value is 1'h0 Bit[6:4]: Delay of lane 3 equals to the value of bit[6:4] × 40 ps, the default value is 3'h0
MIPI Clock delay	16'h3654	8'h00	Bit[3]: Clock invert, the default value is 1'h0 Bit [2:0]: Delay of MIPI clock equals to the value of bit [2:0] × 40 ps. The default value is 3'h0.

9 Sensor Operation

9.1 Illumination Trigger

Mira130 supports an illumination strobe feature and can be used to control a light source (LED or VCSEL). During exposure, the LEDSTROBE pin outputs a logic level 'high' to enable an external illumination.

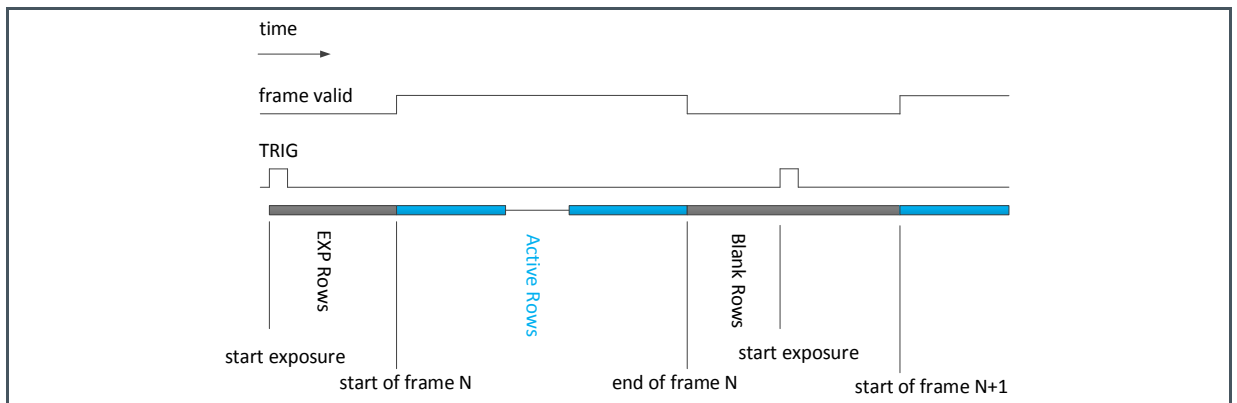
Figure 33:
Illumination Strobe Control Register

Function	Address	Default Value	Description
Illumination strobe enable	16'h3361	8'h00	Bit[7:6]: LED strobe enable 2'b11: LED strobe disable 2'b00: LED strobe enable

9.2 External Triggering Mode

In external triggering mode, the exposure and data output of multiple sensors are synchronized by an external triggering signal applied on the TRIGL pin. When the rising edge of the signal is detected, the chip starts exposure after a short delay, and outputs data after completing exposure. The short delay is determined by register 16'h3226, and the exposure time is determined by registers {16'h3e00[3:0], 16'h3e01, 16'h3e02}. The frame rate is determined by the signal. Figure 34 shows the timing diagram of external triggering mode which consists of the following time intervals: EXP Rows, Active Rows, and Blank Rows.

Figure 34:
External Triggering Global Shutter Mode Timing Diagram



(1) EXP Rows = {16'h3e00[3:0], 16'h3e01, 16'h3e02[7:4]} + 16'h3226, in the unit of line.

- (2) When the rising edge of the TRIG is detected, the chip starts exposure after a short delay which is determined by the value of the register 16'h3226, in the unit of line. As multiple pixel reset operations are carried out during the delay to achieve a high image quality, the value of the register 16'h3226 is recommended to keep unchanged.
- (3) Start of frame N indicates the end of the exposure and the start of outputting data.
- (4) During Active Rows, image data can be read. The duration of Active Rows is controlled by registers, in the unit of line.
- (5) Blank Rows is the blanking time after reading image data. The duration of Blank Rows is controlled by registers, in the unit of line.

When using triggered mode, make sure to set IO_FSYNC_OEN register to 0. This sets the pin to high impedance input and disables any output from the pin.

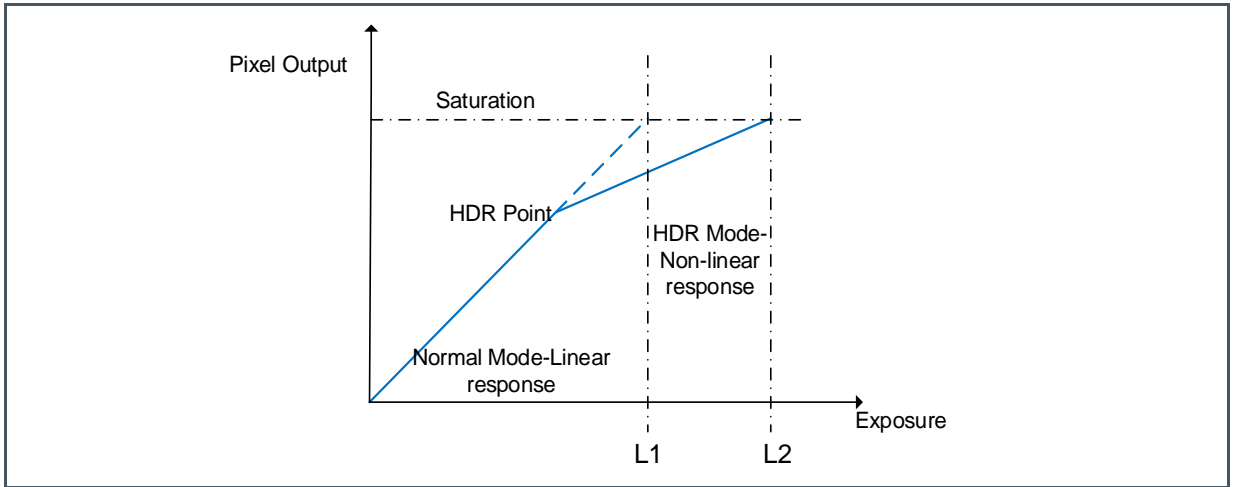
Figure 35:
External Triggering Mode Control Registers

Function	Address	Default Value	Description
External triggering mode enable	16'h3222	8'h00	Bit[1]: External triggering mode enable 1: Enable 0: Disable
Active rows	{16'h3260,16'h3261}	Read only	Active rows = {16'h3260,16'h3261} –
Blank rows	{16'h3228,16'h3229}	{8'h00,8'h02}	Blank rows = {16'h3228, 16'h3229}
IO_fsync	16'h300a	8'h00	bit[2] io_fsync_oen bit[1] io_fsync_sel bit[0] io_fsync

9.3 High Dynamic Range (HDR)

Mira130 provides two exposure modes: Normal mode and High Dynamic Range (HDR) mode.

Figure 36:
Normal and HDR Modes



Under normal mode, as shown in Figure 36, the pixel output value is linear proportional to the exposure time. The maximum exposure time without causing pixel saturation for a given light intensity of an image source is L1. Under HDR mode, as shown in the same figure, for the same light intensity of the image source, the sensitivity of the pixel in HDR mode is the same as normal mode before the pixel output value reaching a HDR point, but is reduced after the HDR point. Hence, the maximum exposure time without causing saturation is L2, implying a higher dynamic range. The dynamic range can be increased by $20 \times \log (L2 / L1)$.

Figure 37:
HDR Mode Timing

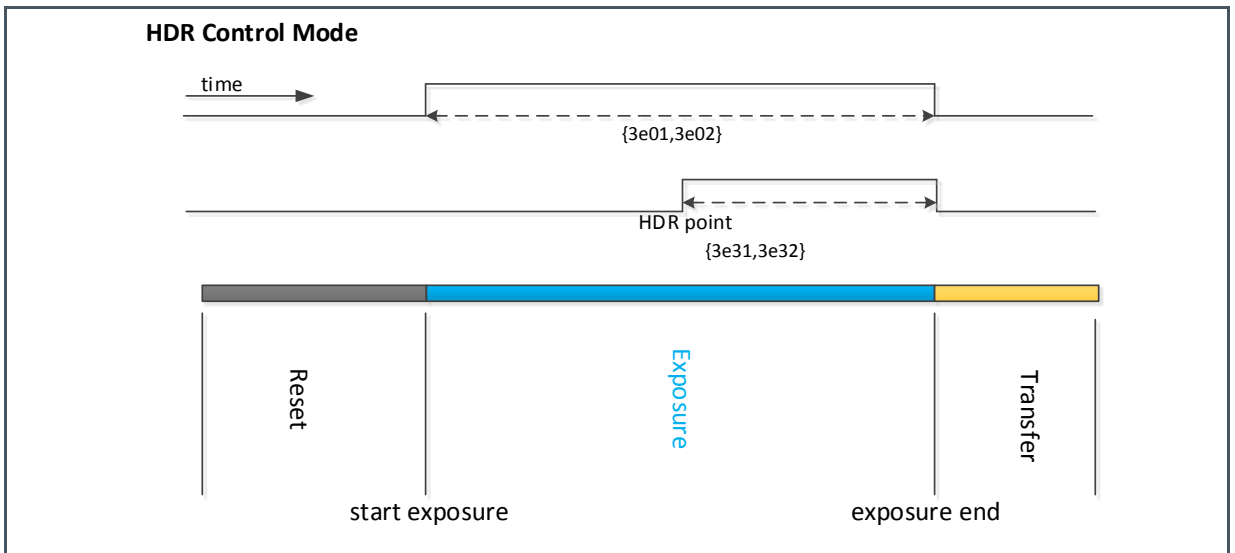


Figure 38:
HDR Mode Control Registers

Function	Address	Default Value	Description
HDR mode enable	16'h3220	8'h83	Bit[6]: HDR mode 1: Enable 0: Disable
Total exposure time	{16'h3e00[3:0], 16'h3e01, 16'h3e02}	20'h00200	In the unit of 1/16 line
HDR exposure time	{16'h3e31, 16'h3e32}	16'h0020	In the unit of 1/16 line
HDRC exposure ratio setting	16'h5400	8'h00	Total exposure time -{16'h3e01, 16'h3e02}; the value of second exposure time {16'h3e31,16'h3e32}, value of 16'h5400=255* (1 – second exposure time/total exposure time)

9.4 AEC & AGC

The AEC/AGC adjustment is based on the image's brightness. AEC adjusts the exposure time while AGC adjusts the gain value so that the image's brightness can fall within a range bounded by pre-set brightness thresholds.

9.4.1 AEC & AGC Control Strategy

This chip does not have the AEC function, so a back-end platform is needed in order to achieve AEC/AGC.

During the AEC/AGC adjustment process, the exposure time and gain are interrelated and should be considered as a whole. A recommended adjustment strategy is as follows: maximize the exposure time first, and then apply gain if the exposure time has reached its maximum.

Consider a dark scene, the sequence of adjustment is: 1) increase the exposure time with no gain until the exposure time reaches its maximum; 2) when the exposure time reaches its maximum but the image is still too dark, adjust the gain. It should be noted that when the gain is increased, the average image noise also increases. However, when the exposure time increases, the signal-to-noise ratio will improve.

On the other hand, when the image is too bright, the gain should be reduced first. If all gains are reduced to their minimum but the image is still too bright, then the exposure time should be reduced.

9.4.2 AEC Control Registers

Figure 39:
Exposure (manual) Control Registers

Function	Address	Description
Exposure time	{16'h3e00[3:0], 16'h3e01, 16'h3e02}	Exposure time under normal mode/ total exposure time under HDR mode, in the unit of 1/16 line
Exposure time under HDR mode	{16'h3e31, 16'h3e32}	In the unit of 1/16 line

For AEC control, please refer to the following instructions:

1. The AEC adjustment step is 1/16 line of exposure time. One line of exposure time equals to line length \times TPCLK, where TPCLK is the period of pixel clock, and line length equals to the value of registers {16'h320c, 16'h320d}.
2. If the exposure time and gain are written to registers in the Nth frame, they are effective on the (N+2)th frame.
3. The upper limit of the exposure time is 0, and the upper limit is frame length - 8 lines, where frame length equals to the value of registers {16'h320e, 16'h320f}. Hence, the minimum value written to registers {16'h3e00[3:0], 16'h3e01, 16'h3e02} is 0, and the maximum value is (the value of registers {16'h320e, 16'h320f} - 8) \times 16.

9.4.3 AGC Control Registers

Figure 40:
Exposure (manual) Control Registers

Mode	ANA GAIN Register	ANA FINE GAIN Register	DIG GAIN Register	DIG FINE GAIN Register
Long exposure time under normal mode/HDR mode	16'h3e08	16'h3e09	16'h3e06	16'h3e07
Short exposure time under HDR mode	16'h3e12	16'h3e13	16'h3e10	16'h3e11

For AGC control, please refer to the following two methods:

1. When register 16'h3e03[3:0] is set to 4'h3, gain equals to the value of {ANA GAIN register, ANA FINE GAIN register } ÷ 8'h20.
2. When register 16'h3e03[3:0] is set to 4'hb, the analog gain and digital can be tuned. In general, the analog gain should be increased first. If the brightness is required to be further increased when the analog gain is increased to the maximum, the digital gain can be increased. The accuracy of the DIG FINE gain of this chip is 1/128.

Figure 41:
Analog Gain Settings

ANA GAIN	ANA FINE GAIN	GAIN Value	dB Value	ANA GAIN	ANA FINE GAIN	GAIN Value	dB Value	ANA GAIN	ANA FINE GAIN	GAIN Value	dB Value
8'h03	8'h20	1.000	0.00	8'h23	8'h31	2.775	8.87	8'h27	8'h3C	6.797	16.65
8'h03	8'h21	1.031	0.27	8'h23	8'h32	2.832	9.04	8'h27	8'h3D	6.910	16.79
8'h03	8'h22	1.063	0.53	8'h23	8'h33	2.889	9.21	8'h27	8'h3E	7.023	16.93
8'h03	8'h23	1.094	0.78	8'h23	8'h34	2.945	9.38	8'h27	8'h3F	7.137	17.07
8'h03	8'h24	1.125	1.02	8'h23	8'h35	3.002	9.55	8'h2F	8'h20	7.250	17.21
8'h03	8'h25	1.156	1.26	8'h23	8'h36	3.059	9.71	8'h2F	8'h21	7.477	17.47
8'h03	8'h26	1.188	1.49	8'h23	8'h37	3.115	9.87	8'h2F	8'h22	7.703	17.73
8'h03	8'h27	1.219	1.72	8'h23	8'h38	3.172	10.03	8'h2F	8'h23	7.930	17.99
8'h03	8'h28	1.250	1.94	8'h23	8'h39	3.229	10.18	8'h2F	8'h24	8.156	18.23
8'h03	8'h29	1.281	2.15	8'h23	8'h3A	3.285	10.33	8'h2F	8'h25	8.383	18.47
8'h03	8'h2A	1.313	2.36	8'h23	8'h3B	3.342	10.48	8'h2F	8'h26	8.609	18.70
8'h03	8'h2B	1.344	2.57	8'h23	8'h3C	3.398	10.63	8'h2F	8'h27	8.836	18.93
8'h03	8'h2C	1.375	2.77	8'h23	8'h3D	3.455	10.77	8'h2F	8'h28	9.063	19.14
8'h03	8'h2D	1.406	2.96	8'h23	8'h3E	3.512	10.91	8'h2F	8'h29	9.289	19.36
8'h03	8'h2E	1.438	3.15	8'h23	8'h3F	3.568	11.05	8'h2F	8'h2A	9.516	19.57
8'h03	8'h2F	1.469	3.34	8'h27	8'h20	3.625	11.19	8'h2F	8'h2B	9.742	19.77
8'h03	8'h30	1.500	3.52	8'h27	8'h21	3.738	11.45	8'h2F	8'h2C	9.969	19.97
8'h03	8'h31	1.531	3.70	8'h27	8'h22	3.852	11.71	8'h2F	8'h2D	10.195	20.17
8'h03	8'h32	1.563	3.88	8'h27	8'h23	3.965	11.96	8'h2F	8'h2E	10.422	20.36
8'h03	8'h33	1.594	4.05	8'h27	8'h24	4.078	12.21	8'h2F	8'h2F	10.648	20.55
8'h03	8'h34	1.625	4.22	8'h27	8'h25	4.191	12.45	8'h2F	8'h30	10.875	20.73
8'h03	8'h35	1.656	4.38	8'h27	8'h26	4.305	12.68	8'h2F	8'h31	11.102	20.91
8'h03	8'h36	1.688	4.54	8'h27	8'h27	4.418	12.90	8'h2F	8'h32	11.328	21.08
8'h03	8'h37	1.719	4.70	8'h27	8'h28	4.531	13.12	8'h2F	8'h33	11.555	21.26
8'h03	8'h38	1.750	4.86	8'h27	8'h29	4.645	13.34	8'h2F	8'h34	11.781	21.42
8'h03	8'h39	1.781	5.01	8'h27	8'h2A	4.758	13.55	8'h2F	8'h35	12.008	21.59
8'h23	8'h20	1.813	5.17	8'h27	8'h2B	4.871	13.75	8'h2F	8'h36	12.234	21.75
8'h23	8'h21	1.869	5.43	8'h27	8'h2C	4.984	13.95	8'h2F	8'h37	12.461	21.91
8'h23	8'h22	1.926	5.69	8'h27	8'h2D	5.098	14.15	8'h2F	8'h38	12.688	22.07

ANA GAIN	ANA FINE GAIN	GAIN Value	dB Value	ANA GAIN	ANA FINE GAIN	GAIN Value	dB Value	ANA GAIN	ANA FINE GAIN	GAIN Value	dB Value
8'h23	8'h23	1.982	5.94	8'h27	8'h2E	5.211	14.34	8'h2F	8'h39	12.914	22.22
8'h23	8'h24	2.039	6.19	8'h27	8'h2F	5.324	14.53	8'h2F	8'h3A	13.141	22.37
8'h23	8'h25	2.096	6.43	8'h27	8'h30	5.438	14.71	8'h2F	8'h3B	13.367	22.52
8'h23	8'h26	2.152	6.66	8'h27	8'h31	5.551	14.89	8'h2F	8'h3C	13.594	22.67
8'h23	8'h27	2.209	6.88	8'h27	8'h32	5.664	15.06	8'h2F	8'h3D	13.820	22.81
8'h23	8'h28	2.266	7.10	8'h27	8'h33	5.777	15.23	8'h2F	8'h3E	14.047	22.95
8'h23	8'h29	2.322	7.32	8'h27	8'h34	5.891	15.40	8'h2F	8'h3F	14.273	23.09
8'h23	8'h2A	2.379	7.53	8'h27	8'h35	6.004	15.57	8'h3F	8'h20	14.500	23.23
8'h23	8'h2B	2.436	7.73	8'h27	8'h36	6.117	15.73	8'h3F	8'h21	14.953	23.49
8'h23	8'h2C	2.492	7.93	8'h27	8'h37	6.230	15.89	8'h3F	8'h22	15.406	23.75
8'h23	8'h2D	2.549	8.13	8'h27	8'h38	6.344	16.05	8'h3F	8'h23	15.859	24.01
8'h23	8'h2E	2.605	8.32	8'h27	8'h39	6.457	16.20	8'h3F	8'h24	16.313	24.25
8'h23	8'h2F	2.662	8.50	8'h27	8'h3A	6.570	16.35	8'h3F	8'h25	16.766	24.49
8'h23	8'h30	2.719	8.69	8'h27	8'h3B	6.684	16.50	8'h3F	8'h26	17.219	24.72
8'h3F	8'h27	17.672	24.95	8'h3F	8'h37	24.922	27.93				
8'h3F	8'h28	18.125	25.17	8'h3F	8'h38	25.375	28.09				
8'h3F	8'h29	18.578	25.38	8'h3F	8'h39	25.828	28.24				
8'h3F	8'h2A	19.031	25.59	8'h3F	8'h3A	26.281	28.39				
8'h3F	8'h2B	19.484	25.79	8'h3F	8'h3B	26.734	28.54				
8'h3F	8'h2C	19.938	25.99	8'h3F	8'h3C	27.188	28.69				
8'h3F	8'h2D	20.391	26.19	8'h3F	8'h3D	27.641	28.83				
8'h3F	8'h2E	20.844	26.38	8'h3F	8'h3E	28.094	28.97				
8'h3F	8'h2F	21.297	26.57	8'h3F	8'h3F	28.547	29.11				
8'h3F	8'h30	21.750	26.75								
8'h3F	8'h31	22.203	26.93								
8'h3F	8'h32	22.656	27.10								
8'h3F	8'h33	23.109	27.28								
8'h3F	8'h34	23.563	27.44								
8'h3F	8'h35	24.016	27.61								
8'h3F	8'h36	24.469	27.77								

Figure 42:
Digital Gain Settings

DIG GAIN	DIG FINE GAIN	Gain Value	dB Value	DIG GAIN	DIG FINE GAIN	Gain Value	dB Value	DIG GAIN	DIG FINE GAIN	Gain Value	dB Value
8'h00	8'h80	1.000	0.00	8'h01	8'hA4	2.563	8.17	8'h03	8'hC8	6.250	15.92
8'h00	8'h84	1.031	0.27	8'h01	8'hA8	2.625	8.38	8'h03	8'hCC	6.375	16.09

DIG GAIN	DIG FINE GAIN	Gain Value	dB Value	DIG GAIN	DIG FINE GAIN	Gain Value	dB Value	DIG GAIN	DIG FINE GAIN	Gain Value	dB Value
8'h00	8'h88	1.063	0.53	8'h01	8'hAC	2.688	8.59	8'h03	8'hD0	6.500	16.26
8'h00	8'h8C	1.094	0.78	8'h01	8'hB0	2.750	8.79	8'h03	8'hD4	6.625	16.42
8'h00	8'h90	1.125	1.02	8'h01	8'hB4	2.813	8.98	8'h03	8'hD8	6.750	16.59
8'h00	8'h94	1.156	1.26	8'h01	8'hB8	2.875	9.17	8'h03	8'hDC	6.875	16.75
8'h00	8'h98	1.188	1.49	8'h01	8'hBC	2.938	9.36	8'h03	8'hE0	7.000	16.90
8'h00	8'h9C	1.219	1.72	8'h01	8'hC0	3.000	9.54	8'h03	8'hE4	7.125	17.06
8'h00	8'hA0	1.250	1.94	8'h01	8'hC4	3.063	9.72	8'h03	8'hE8	7.250	17.21
8'h00	8'hA4	1.281	2.15	8'h01	8'hC8	3.125	9.90	8'h03	8'hEC	7.375	17.36
8'h00	8'hA8	1.313	2.36	8'h01	8'hCC	3.188	10.07	8'h03	8'hF0	7.500	17.50
8'h00	8'hAC	1.344	2.57	8'h01	8'hD0	3.250	10.24	8'h03	8'hF4	7.625	17.64
8'h00	8'hB0	1.375	2.77	8'h01	8'hD4	3.313	10.40	8'h03	8'hF8	7.750	17.79
8'h00	8'hB4	1.406	2.96	8'h01	8'hD8	3.375	10.57	8'h03	8'hFC	7.875	17.93
8'h00	8'hB8	1.438	3.15	8'h01	8'hDC	3.438	10.72	8'h07	8'h80	8.000	18.06
8'h00	8'hBC	1.469	3.34	8'h01	8'hE0	3.500	10.88	8'h07	8'h84	8.250	18.33
8'h00	8'hC0	1.500	3.52	8'h01	8'hE4	3.563	11.04	8'h07	8'h88	8.500	18.59
8'h00	8'hC4	1.531	3.70	8'h01	8'hE8	3.625	11.19	8'h07	8'h8C	8.750	18.84
8'h00	8'hC8	1.563	3.88	8'h01	8'hEC	3.688	11.33	8'h07	8'h90	9.000	19.08
8'h00	8'hCC	1.594	4.05	8'h01	8'hF0	3.750	11.48	8'h07	8'h94	9.250	19.32
8'h00	8'hD0	1.625	4.22	8'h01	8'hF4	3.813	11.62	8'h07	8'h98	9.500	19.55
8'h00	8'hD4	1.656	4.38	8'h01	8'hF8	3.875	11.77	8'h07	8'h9C	9.750	19.78
8'h00	8'hD8	1.688	4.54	8'h01	8'hFC	3.938	11.90	8'h07	8'hA0	10.000	20.00
8'h00	8'hDC	1.719	4.70	8'h03	8'h80	4.000	12.04	8'h07	8'hA4	10.250	20.21
8'h00	8'hE0	1.750	4.86	8'h03	8'h84	4.125	12.31	8'h07	8'hA8	10.500	20.42
8'h00	8'hE4	1.781	5.01	8'h03	8'h88	4.250	12.57	8'h07	8'hAC	10.750	20.63
8'h00	8'hE8	1.813	5.17	8'h03	8'h8C	4.375	12.82	8'h07	8'hB0	11.000	20.83
8'h00	8'hEC	1.844	5.31	8'h03	8'h90	4.500	13.06	8'h07	8'hB4	11.250	21.02
8'h00	8'hF0	1.875	5.46	8'h03	8'h94	4.625	13.30	8'h07	8'hB8	11.500	21.21
8'h00	8'hF4	1.906	5.60	8'h03	8'h98	4.750	13.53	8'h07	8'hBC	11.750	21.40
8'h00	8'hF8	1.938	5.74	8'h03	8'h9C	4.875	13.76	8'h07	8'hC0	12.000	21.58
8'h00	8'hFC	1.969	5.88	8'h03	8'hA0	5.000	13.98	8'h07	8'hC4	12.250	21.76
8'h01	8'h80	2.000	6.02	8'h03	8'hA4	5.125	14.19	8'h07	8'hC8	12.500	21.94
8'h01	8'h84	2.063	6.29	8'h03	8'hA8	5.250	14.40	8'h07	8'hCC	12.750	22.11
8'h01	8'h88	2.125	6.55	8'h03	8'hAC	5.375	14.61	8'h07	8'hD0	13.000	22.28
8'h01	8'h8C	2.188	6.80	8'h03	8'hB0	5.500	14.81	8'h07	8'hD4	13.250	22.44
8'h01	8'h90	2.250	7.04	8'h03	8'hB4	5.625	15.00	8'h07	8'hD8	13.500	22.61
8'h01	8'h94	2.313	7.28	8'h03	8'hB8	5.750	15.19	8'h07	8'hDC	13.750	22.77
8'h01	8'h98	2.375	7.51	8'h03	8'hBC	5.875	15.38	8'h07	8'hE0	14.000	22.92
8'h01	8'h9C	2.438	7.74	8'h03	8'hC0	6.000	15.56	8'h07	8'hE4	14.250	23.08
8'h01	8'hA0	2.500	7.96	8'h03	8'hC4	6.125	15.74	8'h07	8'hE8	14.500	23.23

DIG GAIN	DIG FINE GAIN	Gain Value	dB Value	DIG GAIN	DIG FINE GAIN	Gain Value	dB Value
8'h07	8'hEC	14.750	23.38	8'h0F	8'hC4	24.500	27.78
8'h07	8'hF0	15.000	23.52	8'h0F	8'hC8	25.000	27.96
8'h07	8'hF4	15.250	23.67	8'h0F	8'hCC	25.500	28.13
8'h07	8'hF8	15.500	23.81	8'h0F	8'hD0	26.000	28.30
8'h07	8'hFC	15.750	23.95	8'h0F	8'hD4	26.500	28.46
8'h0F	8'h80	16.000	24.08	8'h0F	8'hD8	27.000	28.63
8'h0F	8'h84	16.500	24.35	8'h0F	8'hDC	27.500	28.79
8'h0F	8'h88	17.000	24.61	8'h0F	8'hE0	28.000	28.94
8'h0F	8'h8C	17.500	24.86	8'h0F	8'hE4	28.500	29.10
8'h0F	8'h90	18.000	25.11	8'h0F	8'hE8	29.000	29.25
8'h0F	8'h94	18.500	25.34	8'h0F	8'hEC	29.500	29.40
8'h0F	8'h98	19.000	25.58	8'h0F	8'hF0	30.000	29.54
8'h0F	8'h9C	19.500	25.80	8'h0F	8'hF4	30.500	29.69
8'h0F	8'hA0	20.000	26.02	8'h0F	8'hF8	31.000	29.83
8'h0F	8'hA4	20.500	26.24	8'h0F	8'hFC	31.500	29.97
8'h0F	8'hA8	21.000	26.44				
8'h0F	8'hAC	21.500	26.65				
8'h0F	8'hB0	22.000	26.85				
8'h0F	8'hB4	22.500	27.04				
8'h0F	8'hB8	23.000	27.23				
8'h0F	8'hBC	23.500	27.42				
8'h0F	8'hC0	24.000	27.60				

9.5 Group Hold

Group hold refers to the packing of a group of registers to be effective at a specific time within a frame. This chip supports a maximum of 4 groups with a total of 320 registers. Each group can be individually controlled (registers packaging, register values writing, and delay setting). The detail of controlling is as follows.

1. Set register 16'h3800 to 8'h0X (X= 0, 1, 2, 3) to start packing group X.
2. Set register 16'h3800 to 8'h1X to end packing group.
3. Set register 16'h3800 to 8'h6X, registers packed in group X are effective immediately.
4. Set register 16'h3800 to 8'h4X, registers packed in group X are effective after N frames, where N is set by a register.



Information

- The maximum number of registers within a group is 16 by default.
- Registers in group X are effective in the (N + 1)th frame when setting register 16'h3800 to 8'h4X.

Figure 43:
Group Hold Control Registers

Function	Address	Default Value	Description
Frame delay control	16'h3817	8'h20	Bit [3:0]: Determine the number of frames to be delayed before the group of registers is effective. Setting to N implies a delay of N frames, and the group of registers is effective in the (N + 1) th frame. Setting to 0 implies no delay and the group of registers is effective in the next frame.
Status control	16'h3800	Write only	Bit[7:0]: Status of group X (X=0,1,2,3) 8'h0X: Start packing group X 8'h1X: End packing group X 8'h6X: Registers in group X are effective immediately 8'h4X: Registers in group X are effective in the (N + 1) th frame, where N is the value of register 16'h3817[3:0]

9.6 HDR Calibration

In order to enhance image quality, this chip supports a HDR calibration (HDRC) feature which can eliminate image noise as a result of using HDR mode. When HDRC is enabled, one more frame named HDR point is read, so the readout time is doubled. Also, there is no exposure during reading when HDRC is enabled. The frame rate is determined by both the exposure time (t_{exp}) and image reading time (t_{read}). For example, if the frame rate is 30 fps under HDR mode (i.e. one frame lasts for 33.33 ms), and t_{read} is 11.11 ms (according to 90 fps), the maximum exposure time is $33.33 \text{ ms} - 2 * t_{read} - 11.11 \text{ ms}$.

Figure 44:
HDRC Control Registers

Function	Register	Default Value	Description
HDR point read enable	16'h3222	8'h00	Bit[5:4]: HDR point 2'b00: HDR point not read 2'b11: HDR point read
HDRC enable	16'h5001	8'h00	Bit[3]: HDRC feature 1'b0: Enable 1'b1: Disable

9.7 Temperature Sensor

The instantaneous temperature of this chip can be measured by an integrated temperature sensor and is stored in a register for reading. The unit is Kelvin, and the accuracy is 0.25 K.

Figure 45:
Temperature Sensor Control Register

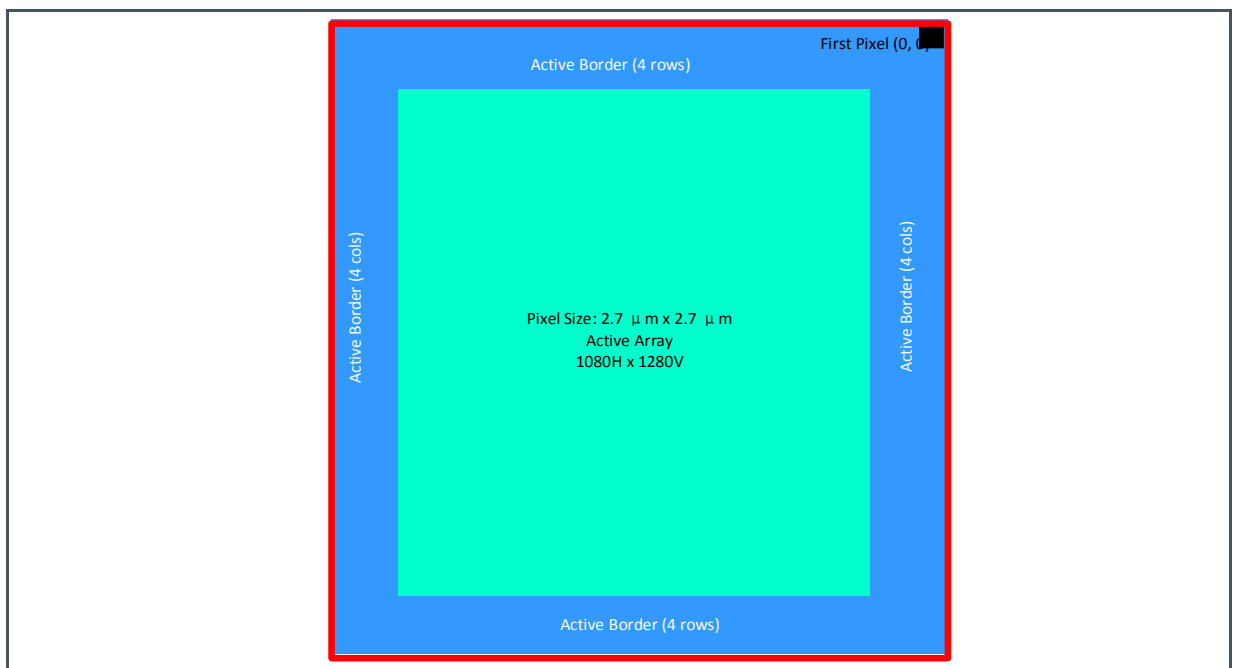
Function	Register	Default Value	Description
Chip temperature	{16'h4c10, 16'h4c11[2:0]}	Read only	Temp [10:0]

9.8 Video Output Mode

9.8.1 Read Order

Figure 46 provides the first read pixel location as well as the entire array structure diagram.

Figure 46:
Mira130 Pixel Array



Mira130 supports mirror mode and flip mode. Mirror mode reverses the sensor data readout order, and flip mode vertically reverses the sensor readout order (as shown in Figure 47). The registers that control these operations are shown in Figure 48.

Figure 47:
Mirror & Flip Examples

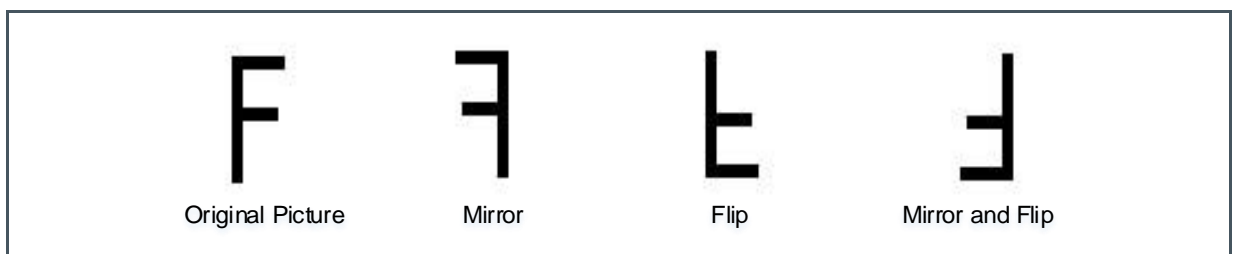


Figure 48:
Mirror & Flip Control Registers

Function	Address	Default Value	Description
Mirror	16'h3221	8'h00	Bit[2:1]: Mirror control 2'b00: Mirror off 2'b11: Mirror on
Flip	16'h3221	8'h00	Bit[6:5]: Flip control 2'b00: Flip off 2'b11: Flip on

9.8.2 Output Window

The table below displays the control registers that define the image window to be read-out.

Figure 49:
Output Window Registers

Function	Address	Default Value	Description
Window width	{16'h3208, 16'h3209}	16'h0438	Output window width
Window height	{16'h320a, 16'h320b}	16'h0500	Output window height
Column start	{16'h3210, 16'h3211}	16'h0010	Output window column start
Row start	{16'h3212, 16'h3213}	16'h0010	Output window row start

9.9 Frame Rate Calculator

The special frame rate of this chip is provided by FAEs. For simplicity, the duration of one line can be calculated as $1/(\text{frame rate} * \text{frame length})$ in seconds.

Figure 50:
Frame Rate Related Registers

Function	Address	Default Value	Description
Frame length	{16'h320e, 16'h320f}	16'h061a	Frame length={16'h320e,16'h320f}

9.10 Test Mode

For the ease of testing, Mira130 provides a grey ramp test mode as shown below.

Figure 51:
Test Mode Image

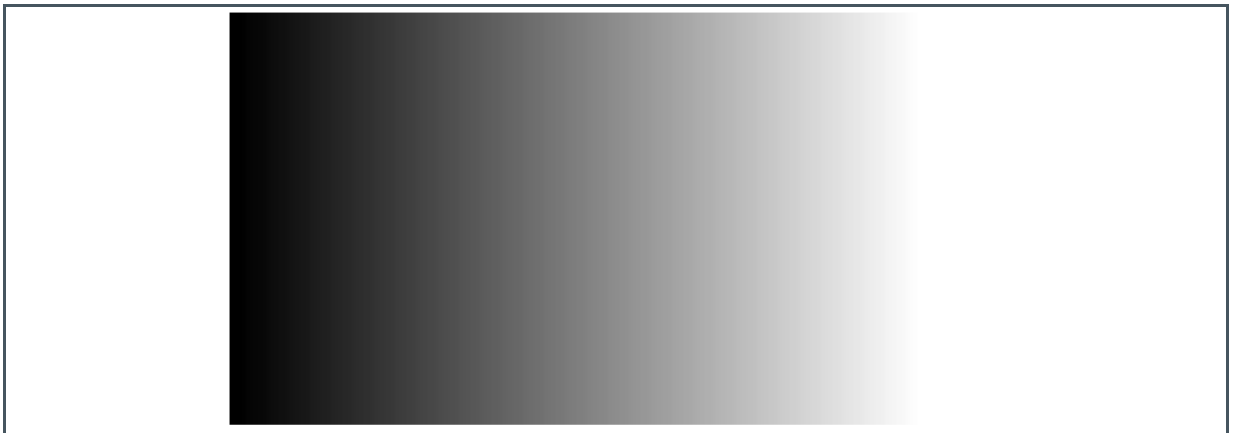


Figure 52:
Test Mode Control Registers

Function	Address	Register Value	Description
Grey ramp mode	16'h4501[3]	1'b1	Bit[3]: Incremental pattern enable 0~ Normal image 1~ Incremental pattern
	16'h3902[6]	1'b0	Bit[6]: blc auto enable 0~ Manual BLC 1~Auto BLC
	16'h391d[2:0]	3'h0	Bit[2:0] : Only open in blc auto mode
	16'h3e06[3:0]	4'hf	Bit[3:0]: Digital gain 4'h0~ 1x 4'h1~ 2x 4'h3~ 4x 4'h7~ 8x 4'hf~ 16x

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